SabreCom-JSP

Rugged Computer System

User Manual

Revision 1.3

Sample illustration; specific models may have different connector arrangements

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Revision 1.3

Contents

Notices

Technical Support

Please use the Technical Support Request form to request assistance with a product you have already purchased.

Product and Sales Inquiry

Please use the Sales Inquiry form to request assistance with selecting a product for your application, or to obtain further information about products and service.

Limited Warranty

Diamond Systems Corporation provides a Limited Warranty for all items in this guide that it manufactures and sells, pursuant to terms provided in the Diamond Systems Corporation Limited Warranty. No other warranty, express or implied, is included. Please download the warranty for additional information.

Trademarks

All trademarks, logos and brand names are the property of their respective owners.

Important Safe Handling Information

WARNING!

ESD-Sensitive Electronic Equipment

- Observe ESD-safe handling procedures when working with this product.
- Always use this product in a properly grounded work area and wear appropriate ESD-preventive clothing and/or accessories.
- Always store this product in ESD-protective packaging when not in use.

Safe Handling Precautions

The Osbourne carrier board contains a high number of I/O connectors with connections to sensitive electronic components. This creates many opportunities for accidental damage during handling, installation, and connection to other equipment.

This section provides critical, best practice suggestions to avoid damage to your products. It includes descriptions of many common causes of damage – all of which can void your warranty.

Please follow these guidelines to be aware of common causes of damage and take the necessary precautions to prevent damage to your Diamond Systems' (or any vendor's) embedded computer boards.

Damage from incorrect handling or storage

- Physical and electronic damage can occur from mishandling. The following are frequent scenarios.
- An electrostatic discharge (ESD) causes a board to malfunction or stop working entirely. If ESD occurs, typically there is no visual sign of damage. While it is often difficult to identify faulty component(s), if the fault is identified there is a good chance that the board can be repaired.
- A screwdriver slips during installation, causing a gouge in the PCB surface and cutting signal traces or damaging components.
- A board is dropped, causing damage to the circuitry near the point of impact. Most of our boards are designed with at least 25 mils clearance between the board edge and any component pad, and ground / power planes are at least 20 mils from the edge. These design rules can minimize but cannot always prevent damage from impact.
- A short occurs when a metal screwdriver tip slips, or a screw drops onto a board while it is powered on. This can cause overvoltage or power supply problems described below.
- A storage rack with slots to hold boards can damage components near the board edge. Many boards have components that are close to the board edge, which are subject to damage in racks.
- Connector pins are bent by improperly dis-assembling attached boards or ribbon cables from a pin header, or from physical impact or improper storage. Typically, bent pins can be repaired one at a time with needle-nose pliers. Severely bent or frequently repaired pins may require the replacement of the connector.

Best Practices to avoid damage during handling or storage

- To prevent ESD damage, always follow proper ESD-prevention practices when handling any electronic components.
- To prevent physical damage from impact, handle all boards with care and work in a safe, spacious environment.
- To prevent short circuit damage from a metallic tool or dropped screw, perform assembly operations ONLY when the system is powered off.

- To prevent damage to fragile components and connector pins in storage, always store boards in individual ESD-safe sleeves in sturdy bins with dividers between boards. Do NOT use racks with slots, or stack boards in a pile or in close proximity.
- To prevent damage to connector pins during assembly or dis-assembly, use caution to align connectors and especially when force is needed to disassemble components and wires. Do not 'rock' connectors back and forth or pull any component at the wrong angle.

Damage due to incorrect voltage or connections

Power supply wired backwards

Diamond Systems power supplies and boards are not designed to withstand a reverse power supply connection. Reverse power will destroy nearly every IC that is connected to the power supply. Reverse power damage is rarely repairable. Check twice before applying power!

Board not installed properly in PC/104 stack

If a PC/104 board is accidentally shifted by 1 row or 1 column (of pins) it is possible for power and ground signals on the bus to contact the wrong pins. For example, this can damage components attached to the data bus because it puts the ±12V power supply lines directly on data bus lines.

Overvoltage on analog input

If a voltage applied to an analog input exceeds the design specification of the board, the input multiplexor and/or parts behind it can be damaged. Most of our boards will withstand an erroneous connection of up to ±35V on the analog inputs, even when the board is powered off, but not all boards, and not in all conditions.

Overvoltage on analog output

If an analog output is accidentally connected to another output signal or a power supply voltage, the output can be damaged. On most of our boards, a short circuit to ground on an analog output will not cause trouble.

Overvoltage on digital I/O line

If a digital I/O signal is connected to a voltage above the maximum specified voltage, the digital circuitry can be damaged. On most of our boards the acceptable range of voltages connected to digital I/O signals is 0-5V, and they can withstand about 0.5V beyond that (-0.5 to 5.5V) before being damaged. However, logic signals at 12V and even 24V are common, and if one of these is connected to a 5V logic chip, the chip will be damaged, and damage may extend past that chip to others in the circuit.

Best Practices to avoid damage due to incorrect voltage or connections

- Ensure all power supply connections are correct and not reversed!
- Ensure all pins are aligned properly before and after assembling boards and components!
- Ensure proper voltage is supplied to all analog inputs!
- Ensure all analog voltage outputs do not connect to another signal output or power supply output!
- Ensure all voltages for digital I/O lines are proper and with range, and that higher voltage signals (24V or 12V) are not supplied to lower voltage circuits (12V or 5V)!

IMPORTANT! Always check twice before Powering Up!

1. Description

1.1. Overview

SabreCom-JSP is Diamond's new rugged platform for applications requiring custom I/O. Three connector positions are provided to support standard I/O options as well as customer specific I/O. High-speed interfaces such as HDMI and USB 3.0 are supported via dedicated connectors. I/O expansion can be provided by a combination of PCIe/104 and PCIe minicard I/O modules.

The system is based on Diamond's Jasper SBC, which utilizes a COM Express CPU core. This design yields several important benefits: The system can be configured for a wide range of performance and power consumption levels by choosing from a variety of pre-qualified COMs. If the currently chosen COM reaches end-of-life, the program's lifetime can be easily extended by selecting a newer one, avoiding the cost and risk associated with purchasing obsolete / EOL products or designing a new system that is backward compatible. Jasper utilizes a thicker PCB (.090" / 2.3mm), latching I/O connectors, and full -40/+85C operating temperature to provide increased ruggedness.

Additional features enhance SabreCom-JSP's ruggedness: Diamond's JMM-7500 DC/DC power supply with MIL-STD-461/704/1275 compliance provides up to 80 watts of isolated power for internal electronics, providing ample capacity for almost any I/O configuration. Rugged D38999 or D38999-style connectors are used for all I/O. The rugged enclosure provides IP67 protection with seals at every joint. Both the embedded processor board and the power supply are conduction-cooled with direct mounting to the top and bottom surfaces of the enclosure. The product is built using the same materials, components, and methods of our Geode systems, which have passed MIL-STD-810H testing (see test results here).

1.2. System Features Overview

The table below lists the standard features available in the system, excluding any additional I/O modules installed for I/O expansion.

Component	Feature
Power	12V DC supply or 9 to 60V DC supply (with Power Filter Board)
CPU	COM Express Module with Intel Core i7 / Xeon processor, 32GB - 96GB RAM, and ECC option (see details below)
Display	1 HDMI Interface
Ethernet	2x 1Gbps
USB	2x USB2.0, up to 3x USB3.0
Digital I/O	Up to 22 with DAQ option; includes 8 counter/timers and 4 PWMs
Analog I/O	16 16-bit inputs, 4 16-bit outputs, with DAQ option
Serial Port	4x RS-232 / RS-422 / RS-485 (jumper configurable in pairs)
Audio	Stereo in, Stereo out, mono Mic in
Utility	I2C, SPI, Reset, & Power Button
Expansion IO	▪ 2 PCIe minicard sockets with PCIe and USB connectivity ▪ 1 PCIe/104 socket supporting 1 PCIe x1 interface I/O module (can also be used to install a PCIe minicard carrier with 4 additional minicard sockets) ▪ 3 front panel cutouts available for I/O expansion, utilizing any combination of D38999 or USB3FTV connectors

1.3. Processor and RAM

SabreCom-JSP is available with a selection of Intel processors and RAM capacity. The processor is provided by a COM Express Type 6 COM (computer on module) mounted on Diamond's Jasper SBC. COMs may be added to or removed from the list of available options, so check the website or contact Diamond Systems Sales department for the current list. As of the date of this manual, the following options are available:

Generation	Class	Processor	RAM	ECC
11 "Tiger Lake"	Core i7	1185GRE	32GB soldered	No
11 "Tiger Lake"	Core i7	1185G7E	32GB / 64GB SODIMM	No
11 "Tiger Lake"	Xeon	11865MRE	32GB SODIMM	Yes
11 "Tiger Lake"	Xeon	11865MRE	32-96GB SODIMM	No
13 "Raptor Lake"	Core i7	1365URE	32-64GB	No

Processor approximate performance ratings are listed below.

Note: PassMark ratings are determined by Passmark.com and are only indicative of relative performance. Actual performance can only be determined by using the product in the intended application.

Generation	Type	Processor	PassMark* (approx.)	Max RAM
11 Tiger Lake	Core i7	1185GRE	8,000	32GB
11 Tiger Lake	Core i7	1185G7E	10,300	64GB
13 Raptor Lake	Core i7	1365URE	10,300	64GB
11 Tiger Lake	Xeon	11865MRE	19,600	96GB or ECC 32GB

1.4. I/O Connectors

1.5. General

SabreCom-JSP contains 6 connectors for power and I/O. The left three connectors J1, J2, and J3 are non-configurable, and are used for power input and all standard SBC I/O including HDMI, gigabit Ethernet, USB 2.0, serial ports, audio and utility signals. Connectors J4, J5 and J6 are user configurable.

The single board computer used in SabreCom-JSP (Jasper) is available with a built-in data acquisition circuit. With this option, J4 is used for analog I/O and J5 for digital I/O, leaving J6 free for a USB 3.0 connector or other I/O, as shown in the below illustration.

Ref Des	J1	J2	J3	J4	J5	J6
Function	Power in	HDMI	2x GbE, 2x USB 2.0, 4x Serial, Audio, Utility	Expansion (Analog I/O) or USB 3.0	Expansion (Digital I/O) or USB 3.0	Expansion or USB 3.0
Connector	38999/C	SJT 19	38999/F	38999/D 38999/E USB3FTV	38999/D 38999/E USB3FTV	38999/D 38999/E USB3FTV

B1: Power button
A1, A2: SMA connector locations

Figure 1-1: I/O connector configuration with data acquisition and 1 USB 3.0 port

1.6. Connector Configuration Options

In a system without the built-in data acquisition circuit, expansion I/O connectors J4, J5 and J6 can be fitted with any combination of D38999 D or E size connectors or USB3FTV USB-3.0 capable connectors. Custom front panel designs can also be provided if different size or style connectors are needed.

Standard configuration options include:

Figure 1-2: Standard I/O connector configuration options for J4, J5 and J6

1.7. Connector Caps

Each connector is accompanied by a cap. In most cases the cap is attached by a cable or chain to the front face. A sample illustration is shown below using a system with 3 USB 3.0 expansion connectors.

1.8. Antennas

SabreCom-JSP contains front panel cutouts (labeled A1 and A2) to support up to 2 SMA connectors for a modem or other communications module. If either cutout is not populated with an antenna, a dummy connector with cap is installed.

1.9. Control Button

A front panel momentary switch (push to make, release to break) labeled B1 provides a configurable control button. The default function is PC Power Button. A short press will turn power on, and a long press will turn power off. On request the button can be wired for Reset function.

1.10. I/O Expansion Boards

I/O expansion can be realized via PCIe/104 and PCIe / USB minicard expansion modules. A maximum of 2 minicards + 1 PCIe/104 module can be accommodated simultaneously. If the PCIe/104 board is a minicard adapter, up to 6 minicards can be installed. Both Diamond and third-party I/O boards can be used.

The standard height enclosure can support up to 2 minicards. A taller enclosure is required to add more than 2 minicards or any PCIe104 module. See the Mechanical Drawing section for further details.

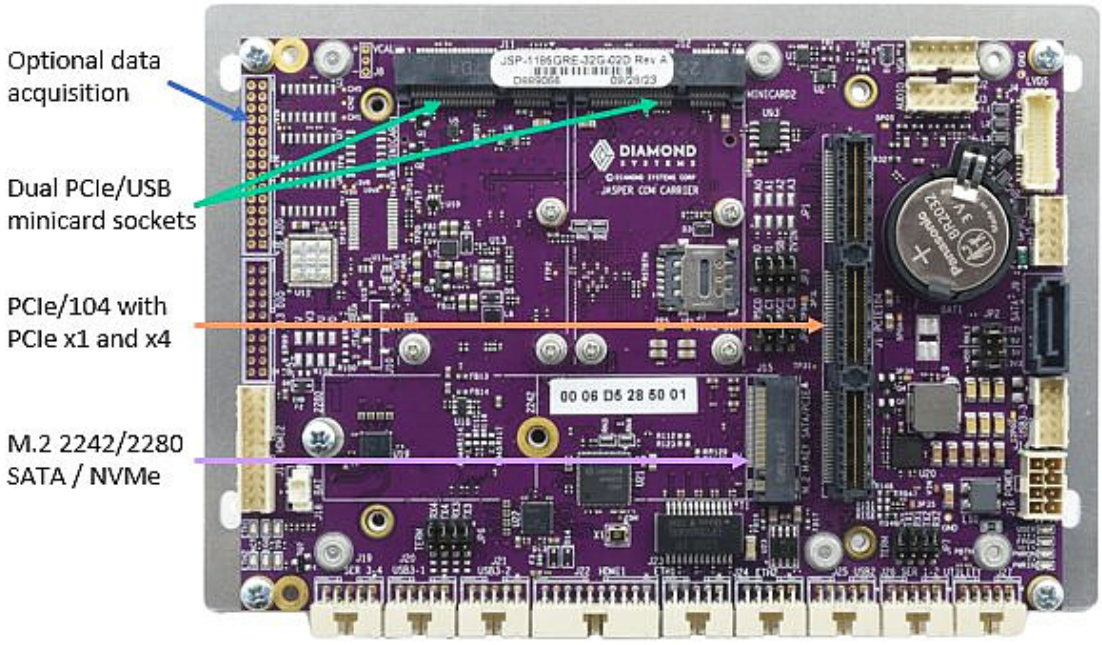


Figure 1-3: PCIe/104 I/O Expansion Board

The minicard sockets support both full-size (51mm length) and half-size (27mm length) minicards. Both PCIe x1 and USB2.0 interfaces are provided on each socket. The interface is auto-detected by the SBC; no manual or BIOS configuration is required. SabreCom systems are generally preconfigured at the factory with the customer's choice of minicards, however you can also install your own minicard.

Common I/O expansion types available include (quantities shown are per installed I/O card):

- Serial ports: 4 RS-232/422/485 ports with optional isolation per minicard, or 8 ports via PCIe/104 module
- CAN: single, dual, and quad isolated CAN via minicard
- Ethernet: one 1GbE or 2.5GbE port via minicard
- USB 3.0: The Jasper SBC used in SabreCom-JSP contains 3 USB 3.0 ports. Any or all of them can be brought out to the front panel as needed.

- MIL-STD-1553: dual redundant ports available via minicard
- Digital I/O: up to 36 I/O via minicard or 22 GPIO via optional integrated DAQ circuit on Jasper SBC
- Analog I/O: 8 16-bit inputs and 4 16-bit outputs, along with 16 GPIO, per minicard, or 16 16-bit inputs and 4 16-bit outputs via optional integrated DAQ circuit on Jasper SBC

1.11. Mass Storage

Mass storage is provided via an M.2 M-Key socket supporting both 2242 and 2280 size modules. Both NVMe (PCIe x1) and SATA interfaces can be supported depending on the selected COM. All standard configurations utilize M.2 SATA SSDs up to 2TB in capacity.

The Jasper SBC used in SabreCom-JSP also provides an industry-standard 7-pin SATA connector for use with externally mounted drives. This connector is unused in all standard product configurations, and using it requires the installation of a custom mounting bracket for the external drive.

1.12. Operating System Support

The operating system is installed on an M.2 M-Key SATA solid state disk installed on the Jasper board. The SATA disk capacity can range from 512GB to 2TB based on the ordered configuration.

Operating System Support
Windows 10 – 64 Bit
Ubuntu Linux – 64 Bit

1.13. Mechanical, Electrical, Environmental

Mechanical, Electrical and Environmental Properties	
Dimensions	▪ Standard height enclosure: 10.0”W x 8.4”D x 3.1”H / 254mmW x 214mmD x80mmH ▪ Tall enclosure: 10.0”W x 8.4”D x 4.1”H / 254mmW x 214mmD x 103mmH
Cooling	▪ Conduction Cooling for internal electronics ▪ Convection cooling for overall system
Power input	▪ +12V DC / 18-30VDC with MIL-STD-461 filter option ▪ 9-60VDC with MIL power supply option
Operating Temp	▪ -40°C to +75°C
Weight	▪ Base model (no installed I/O): 3.22 Kg / 7.10 lbs. ▪ System weight is dependent on installed options

1.14. Power Supply

SabreCom-JSP supports two power path options:

1. A MIL-STD-461 rated power filter board can be installed. With this filter, the input voltage for the system must be pre-selected for either 12VDC input +/- 5% or 18-36VDC input. If this filter is installed, it will be mounted on top of the Jasper SBC.
2. Diamond's rugged JMM-7500 series power supply with 80W output capacity can be installed to provide MIL-STD-461, -704, and -1275 compliance, along with input to output isolation. With this power supply installed, the input voltage range is 9-60VDC. This power supply provides a nominal output voltage of 24VDC to power the Jasper SBC and any other independent boards in the system. If this power supply is installed, it will be mounted on the bottom lid of the system so its heat can be dissipated through its integrated heat spreader directly into the bottom lid. Direct mounting the relatively heavy power supply to the case also creates a more rugged assembly resistant to shock and vibration.

Any installed I/O modules (minicards or PCIe/104 boards) obtain their power directly from the Jasper SBC via their sockets. These sockets provide the required standard power supply voltages (3.3V and/or 5V) regardless of the system input voltage.

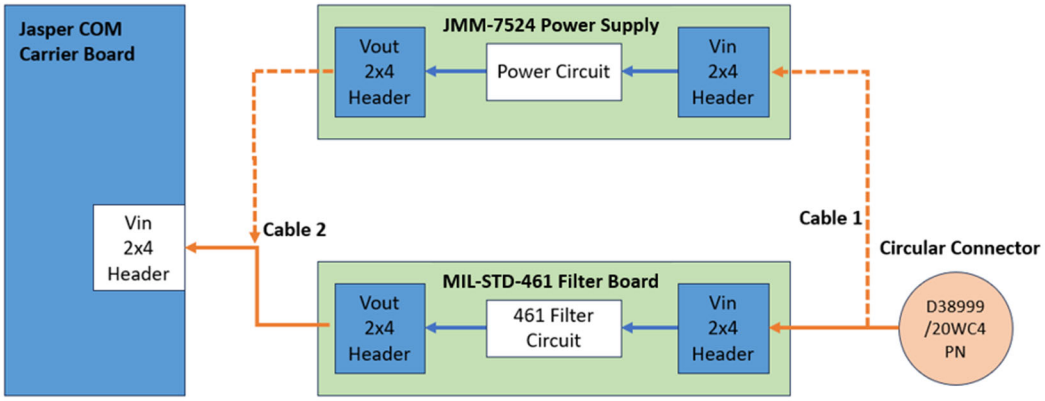


Figure 1-4: Power suppy options

1.15. Backup Battery

A 3.3V nominal CR2032 socketed coin cell battery mounted on the Jasper board in the system provides backup for the real-time clock (RTC) when the system is powered off. This battery has a calculated lifetime of over 5 years when the system is unpowered. The system can boot and function normally without a backup battery as well. Replacement of the battery requires opening up the system. Turn the unit upside down, remove the screws holding the bottom cover in place, remove the bottom cover, and the battery will be visible on the top side of the Jasper board. A CR2032 can be used in place of the BR2032, although its higher self-discharge rate will result in shorter lifetime.

1.16. Display

The board offers one HDMI video output via a rugged SJT connector. This connector is capable of supporting up to 2K/60 or 4K/30 video output.

1.17. Audio Interface

The system provides standard PC Analog Audio Line In, Line Out, and Mic signals on rugged circular connector J3.

1.18. Serial Ports

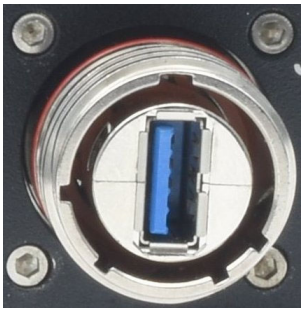
The system supports 4 serial ports derived from the COM installed on the Jasper SBC. The ports use SP336 transceivers (1 transceiver for 2 ports) to support RS-232, RS-422, and RS-485 protocols. The protocol is selected in pairs (ports 1&2 and ports 3&4) using jumpers on the Jasper SBC. The system ships with these ports preconfigured to the customer's request. On board jumpers are provided to enable 121-ohm line termination for RS-422 and RS-485 protocols. All jumpers can be replaced with soldered 0-ohm resistors to enhance ruggedness and reliability.

All serial ports have fail-safe operation to prevent oscillation on unconnected inputs. Differential receivers (RS-422 and RS-485) will default to a logic 1 if inputs are floating or shorted. All serial port outputs and inputs are protected from ESD strikes up to +/-15KV.

1.19. USB

By default, the system supports 2 USB2.0 ports routed to rugged I/O connector J4.

Depending on the selected configuration, up to 3 USB 3.0 ports may also be available. These ports are exposed on the front panel with a USB3FTV connector, consisting of a rugged MIL-DTL-38999 style shell with a USB 3.0 Type A socket insert. The photo below shows this connector.



1.20. PCIe104 Expansion

The board offers PCIe/104 expansion with a full-size 3-bank PCIe104 connector on the Jasper board. The connector used has the taller 22mm stacking height to ensure sufficient space underneath it to install minicards and their associated cabling.

The connector supports 2-4 PCIe x1 links on the first bank, depending on the installed COM. All COMs support at least 2 links, and some support 4.

The socket may support 1 PCIe x4 link on the 2nd bank of the connector. The availability of this x4 link is dependent on the design of the COM. Please contact Diamond Systems if this x4 link is needed.

PCIe/104 boards obtain power from the PCIe/104 connector. In accordance with the PCIe/104 specification, Jasper provides +5VDC power on banks 1 and 2 of the connector and +12VDC power on bank 3.

Installation of a PCIe/104 board in SabreCom-JSP requires the taller case.

1.21. Utility Signals

Power button, Reset, and I2C signals are available on the circular connector J3. Either the power or reset function can also be routed to the front panel momentary switch. Regardless of the front panel switch function, both functions are available on I/O connector J3.

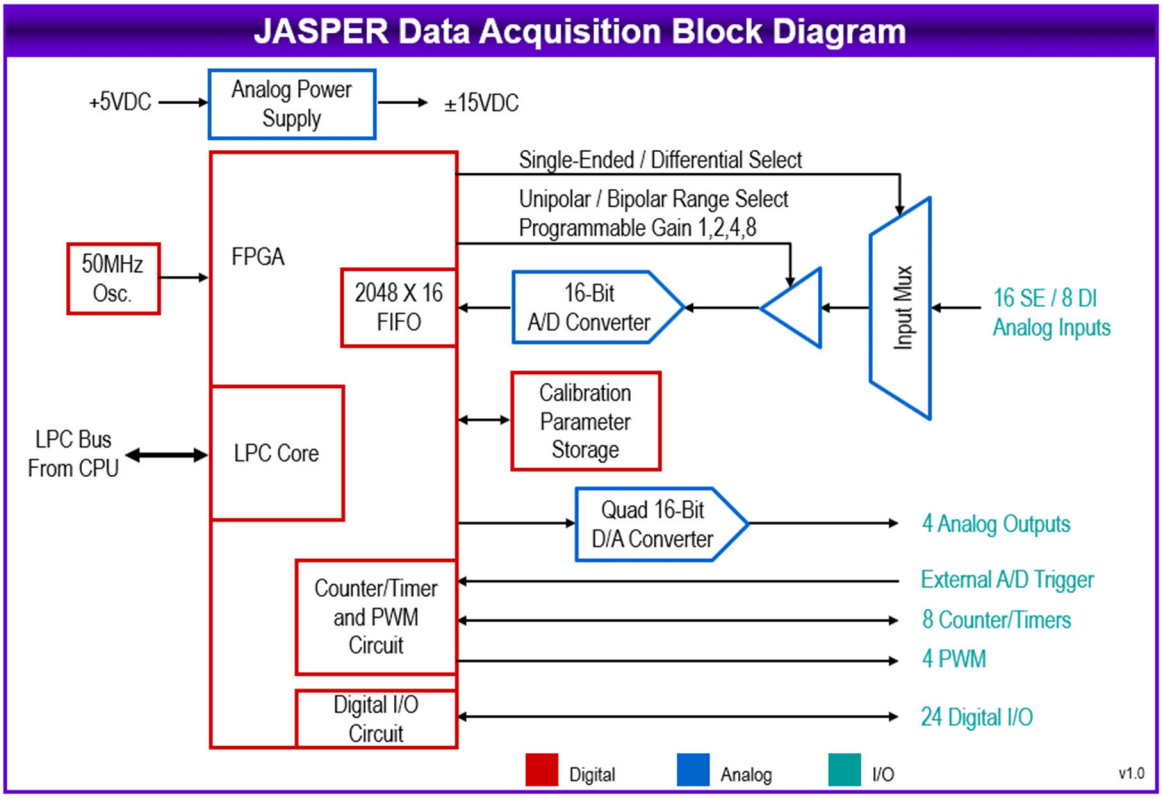
1.22. Trusted Platform Module (TPM)

The board contains an Infineon SLB 9670XQ2.0 TPM module featuring a fully TCG TPM 1.2/2.0 standard compliant module with an SPI interface to the processor. TPM can be used as a root of trust for platform integrity, remote attestation, and cryptographic services.

1.23. Data Acquisition

An optional data acquisition (DAQ) circuit can be installed on the Jasper SBC to provide analog input, analog output, and digital I/O features. Features of the DAQ subcircuit include: 16 single-ended / 8 differential analog inputs with 16-bit resolution, programmable input ranges, and 250KSPS maximum throughput; 4 analog outputs with 16-bit resolution and programmable output ranges; and 22 digital I/O lines with selectable 3.3V/5V logic levels, selectable pull-up/down resistors, programmable direction, buffered I/O, and capability for use as counter/timer and PWM circuits. All features are controlled by Diamond's Universal Driver programming library for C language programming. This DAQ circuit does not affect the availability of the minicard and PCIe/104 expansion sockets. All expansion sockets remain available if the DAQ circuit is installed.

If this option is installed, the I/O signals are made available on the IO connectors J4 and J5. See the dedicated data acquisition chapter later in this manual for more details on this circuit.



2. Block Diagram

The following illustration is a block diagram of the SabreCom-JSP system. The 3 Flex I/O connectors can be connected to any combination of analog and digital I/O from the Jasper SBC, minicards installed on Jasper, installed PCIe/104 module (or minicards on a PCIe/104 minicard adapter), or USB 3.0 connectors on the Jasper SBC. In the maximum I/O configuration, up to 165 I/O contacts are available with 3x E size D38999 connectors.

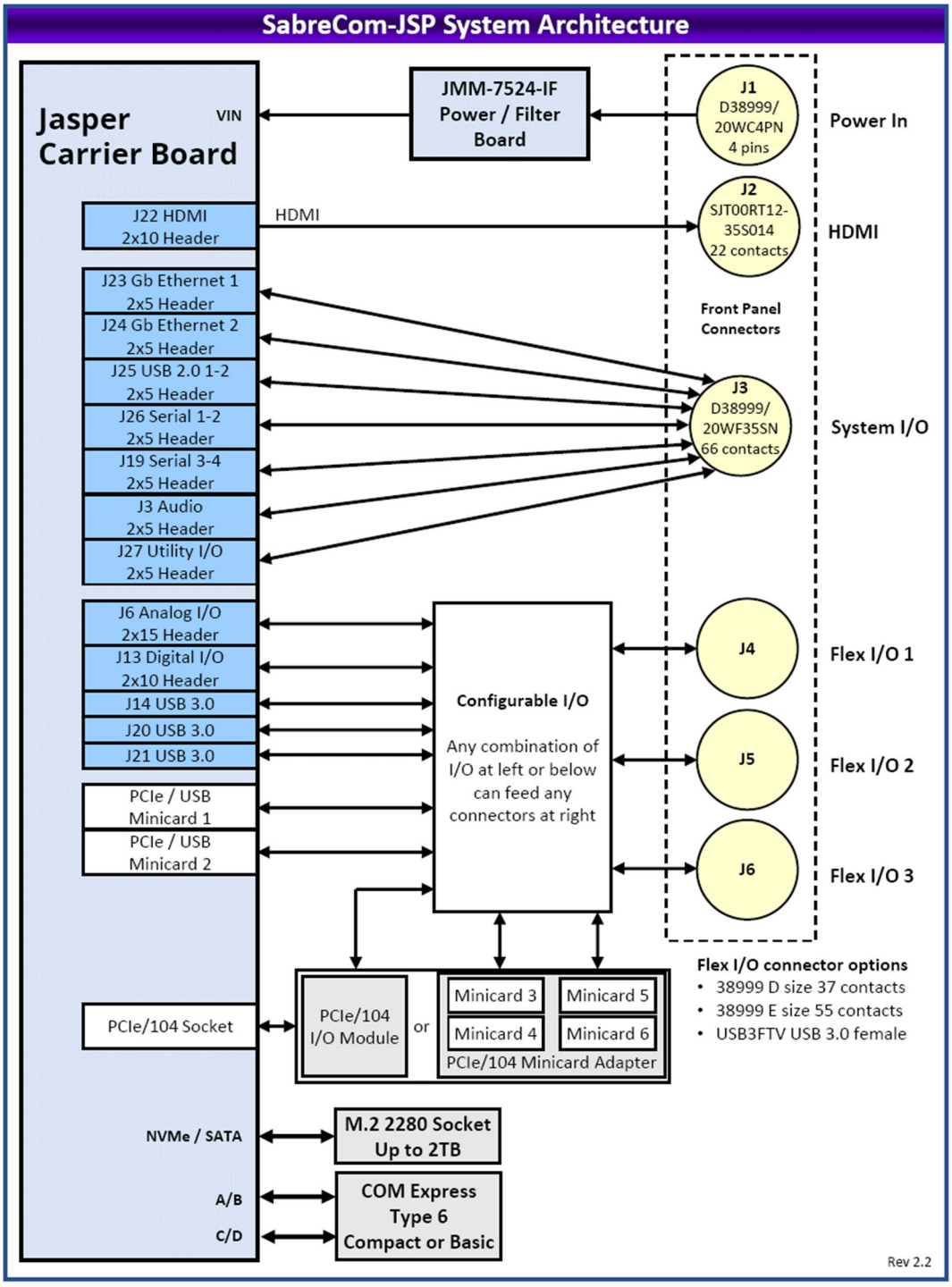


Figure 2-1: System Architecture of SabreCom-JSP

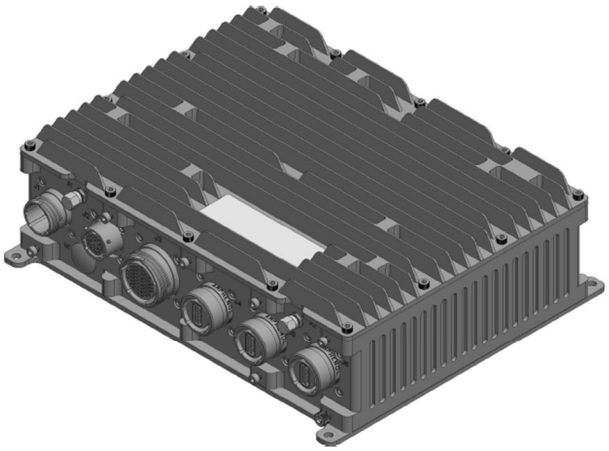
3. Mechanical Drav

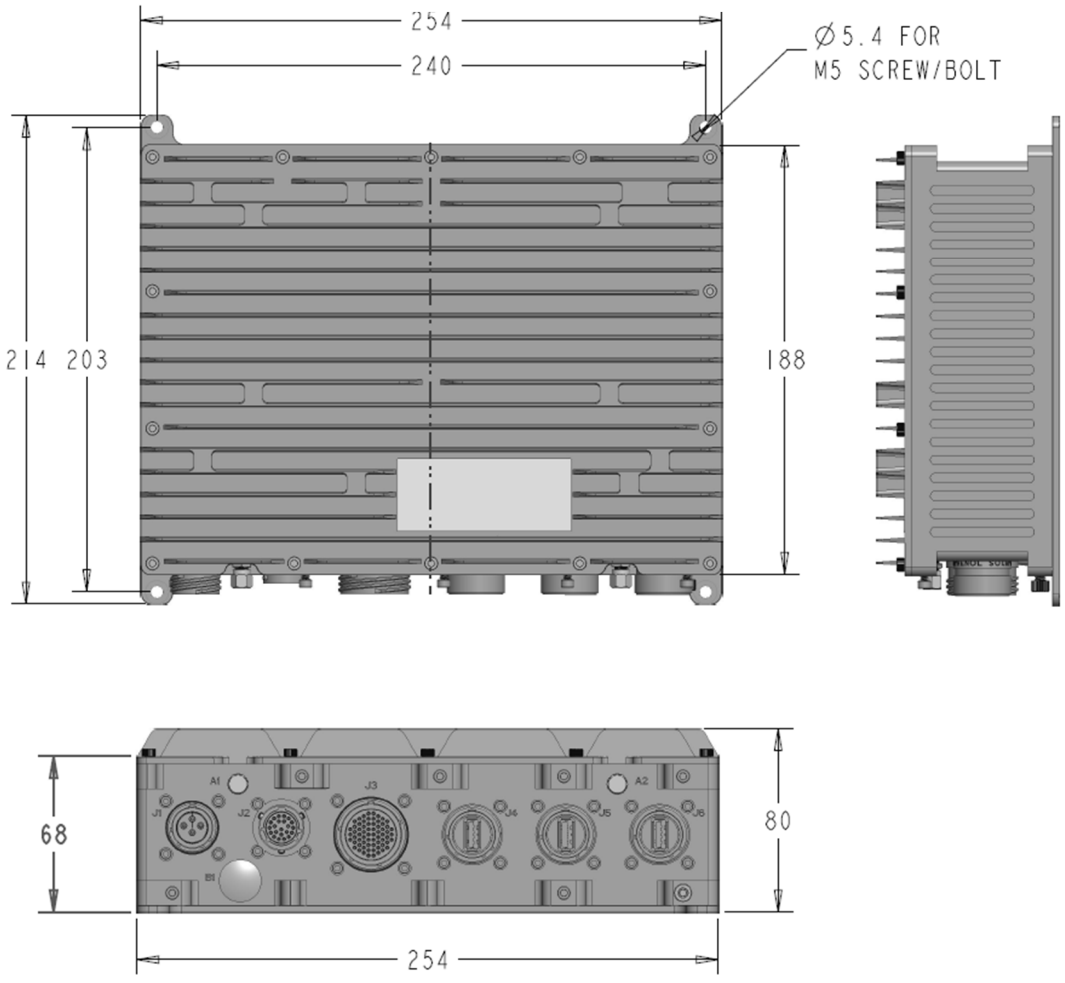
3.1. Overall Dimension

3.1.1. Standard Height Encl

The standard height enclosure t support the installation of a PCIe/104 module. It has the fo

- 10.0”W x 8.4”D x 3.1”H



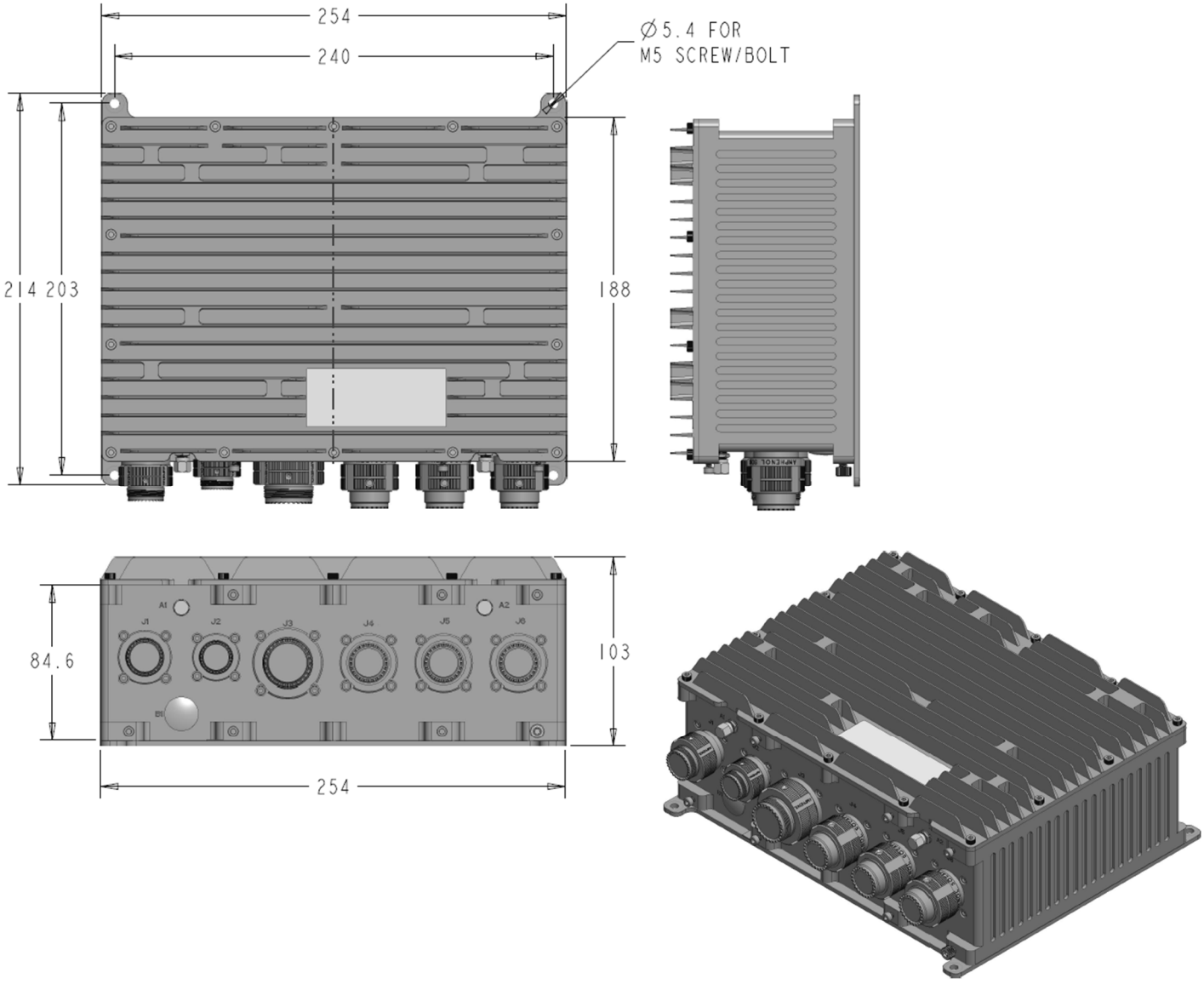


Standard height enclosure (No PCIe/104 module)

3.1.2. Taller Height Enclosure

To add more than 2 minicards or any PCIe104 module, a taller enclosure is required. (Adding more than 2 minicards requires the use of a PCIe/104 minicard adapter, which can support up to 4 additional minicards.) The default taller height enclosure has the following dimensions. Custom heights are also available if needed.

- 10.0”W x 8.4”D x 4.1”H / 254mmW x 214mmD x 103mmH



Taller height enclosure (supports 1 PCIe/104 module)

3.2. Detailed Drawings

Top-down mechanical drawings of the bottom lid, mid-body, and top lid are given below.

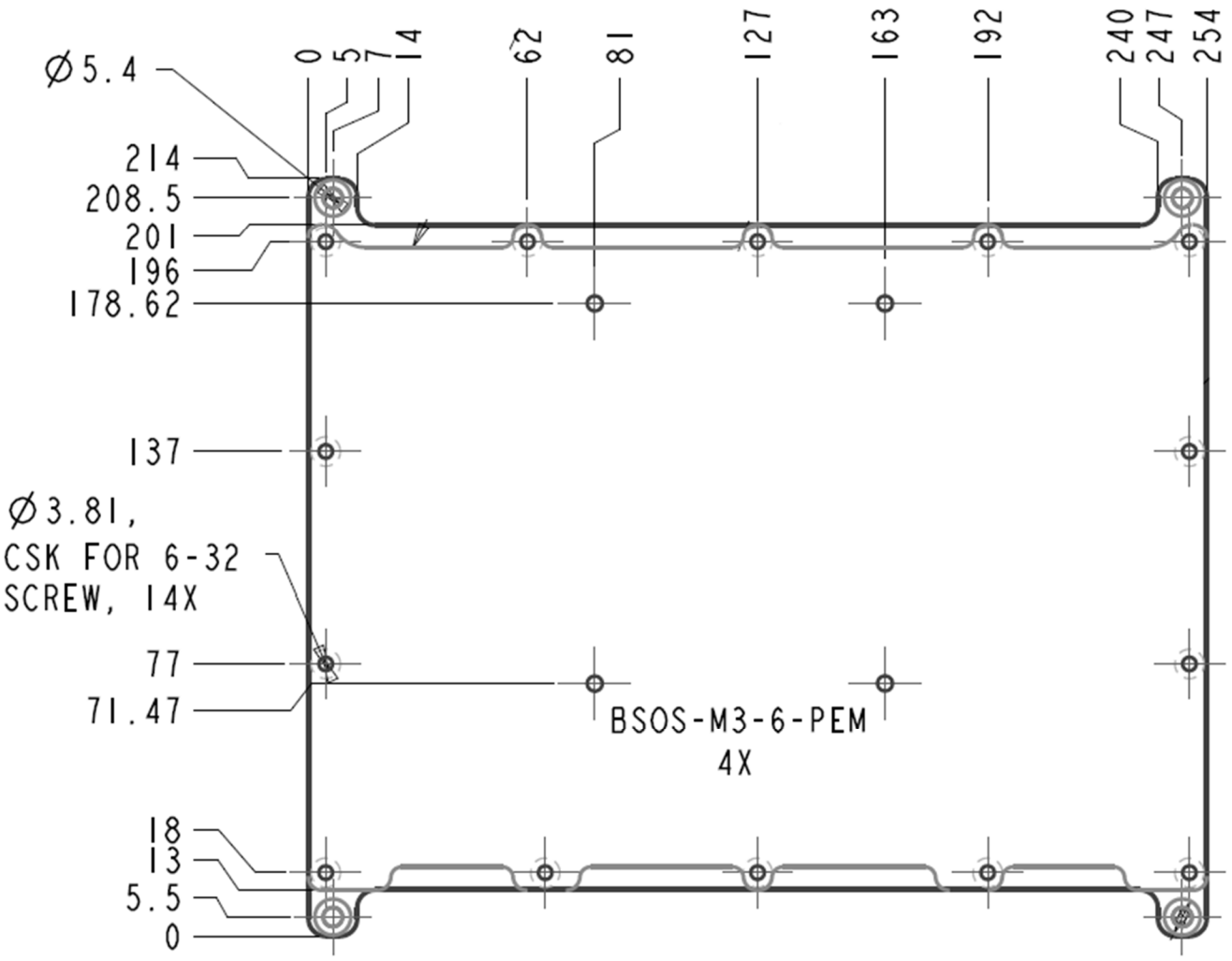


Figure 3-1: Mechanical outline, bottom lid

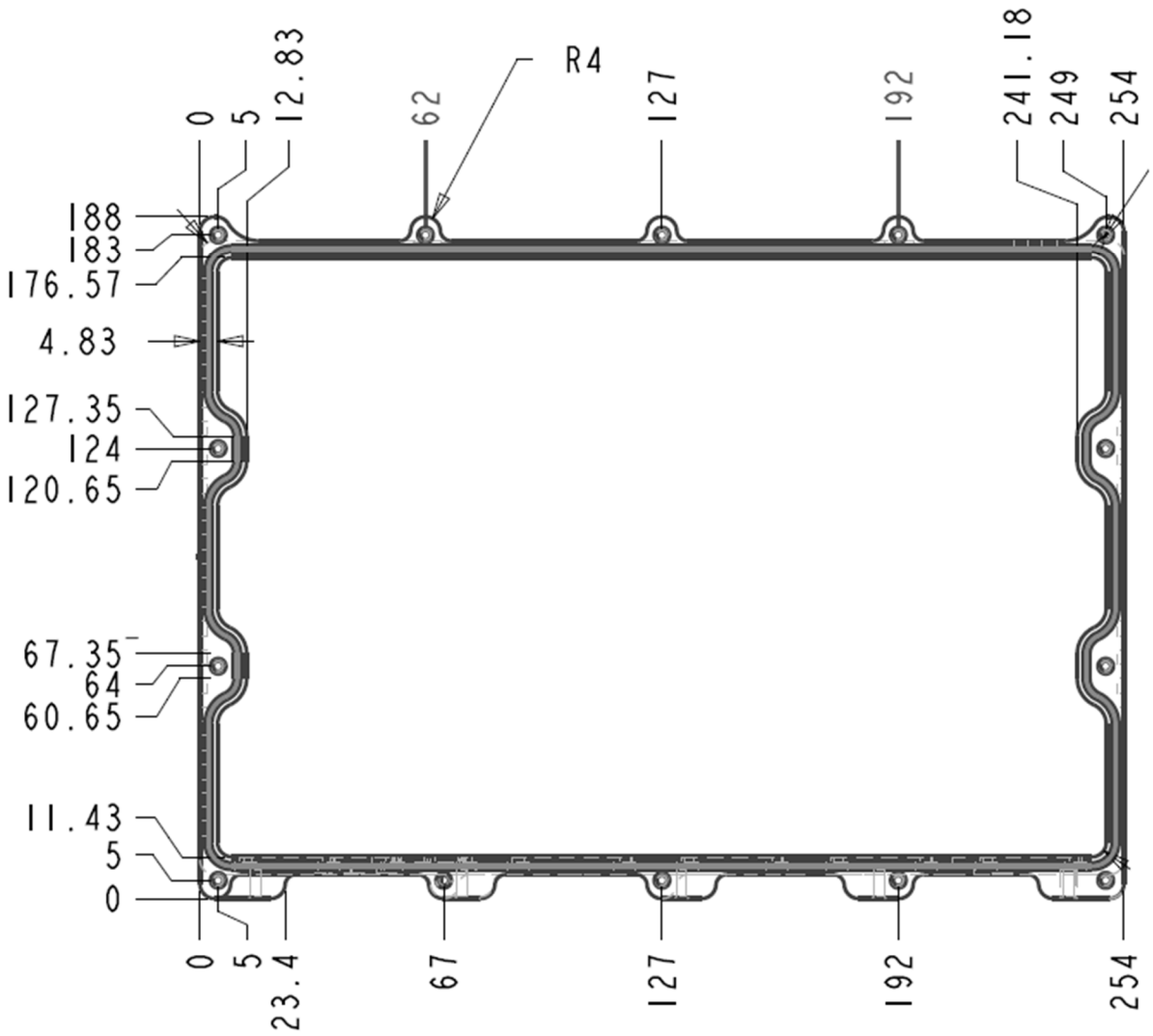


Figure 3-2: Mechanical outline, enclosure body

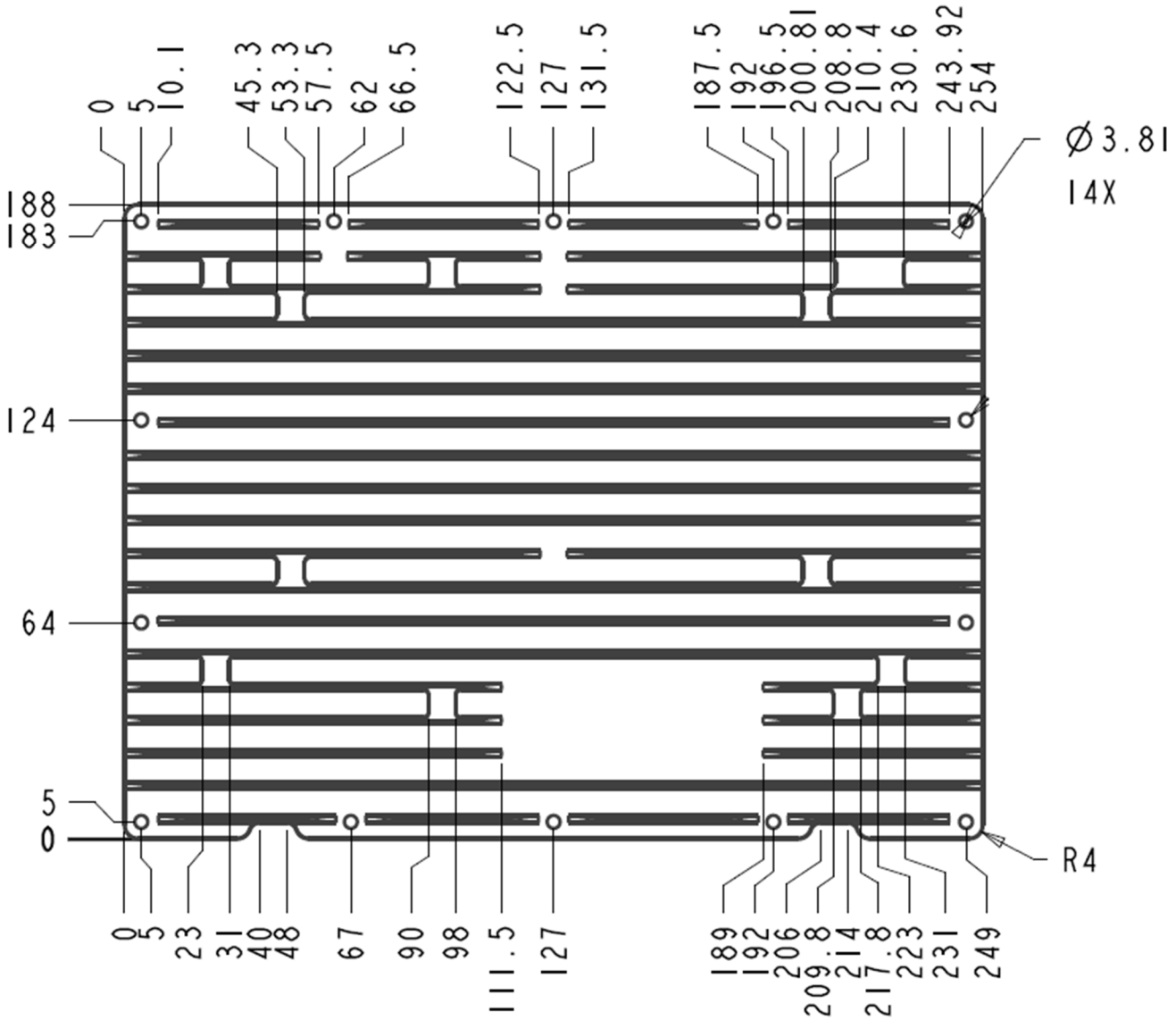


Figure 3-3: Mechanical outline, top view

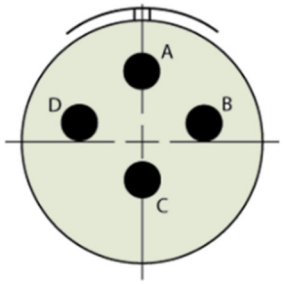
4. Standard I/O Connectors

SabreCom-JSP contains 3 standard I/O connectors for input power, HDMI display, and system I/O. These connectors are described here. The 3 Flex I/O connectors are described in the next chapter.

All 3 standard connectors are installed from the inside of the box with sealing gaskets and nut plates and fixed in place with 4-40 socket head sealing screws.

The system includes caps for all connectors.

4.1. J1 - Power Input

Connector type	**MIL D38999/20WC4PN**	
Description	Shell type	Wall Mount Receptacle
	Material and finish	Olive Drab Cadmium
	Shell Size	C
	Insert Arrangement	C4
	Contact type	Pin
	Keying position	Normal Keying
Illustration ▪ Viewed from rear of panel mount connector (Terminal Insertion Side) ▪ Viewed from front of mating connector		

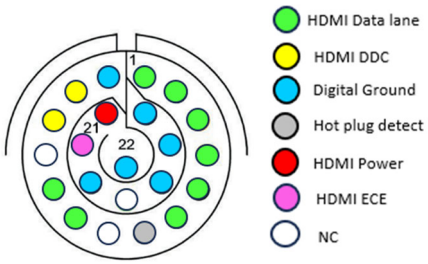
Connector Pinout

Number of wires in cable: 4, No. of positions used: 4, No. of positions unused: 0

Diamond Systems mating cable part no.: 6987092

D38999 Pin no.	**Signal**
A	Ground
B	Ground
C	Vin
D	Vin

4.2. J2 – HDMI

Connector type	MIL SJT00RT12-35DS014	
Description	Shell type	Straight Socket
	Material and finish	Cadmium plated
	Shell Size	B
	Insert Arrangement	12-35 (22 contacts)
	Contact type	Socket
	Keying position	Normal Keying
Illustration ▪ View from pin insertion side of wall mount connector ▪ View from mating face of mating connector		

Connector Pinout

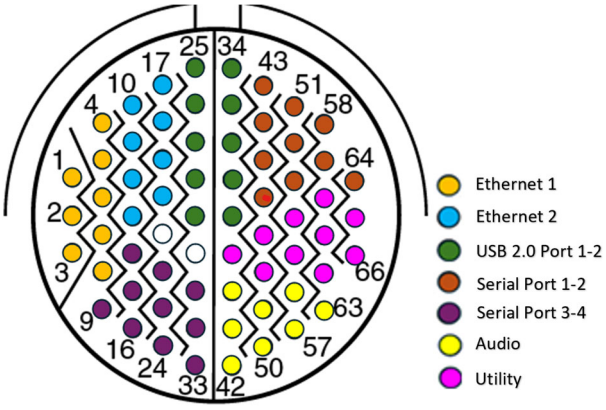
Twisted pairs are indicated by ovals. Customer cables must adhere to twisting requirements for proper operation.

Diamond Systems mating cable part no.: 6987095

SJT Pin no.	Signal	HDMI pin no.
1	HDMI_DP2_TX0_CON_P	1
2	HDMI_DP2_TX0_CON_N	3
15	GND_DIG	2
3	HDMI_DP2_TX1_CON_P	4
4	HDMI_DP2_TX1_CON_N	6
16	GND_DIG	5
5	HDMI_DP2_TX2_CON_P	7
6	HDMI_DP2_TX2_CON_N	9
17	GND_DIG	8
9	HDMI_DP2_TX3_CON_P	10
10	HDMI_DP2_TX3_CON_N	12
19	GND_DIG	11
20	HDMI_CEC_CON	13
12	HDMI_SCL_CON	15
13	HDMI_SDA_CON	16
14	GND_DIG	17
21	V_5P0_HDMI	18
7	HDMI_HPD_CON	19
22	GND_DIG	NC
11	GND_CHASSIS	NC
18	GND_CHASSIS	NC

SJT Pin no.	Signal	HDMI pin no.
8	NC	NC

4.3. J3 - 2x Ethernet, 2x USB 2.0, 4x Serial, Audio, Utility

Connector type	MIL D38999/20WF35SN
Description	Shell type Straight Socket Material and finish Olive Drab Cadmium Plated Nickel Base Shell Size F Insert Arrangement F35 Contact type Pin Keying position Normal Keying
Illustration Front view of pin insert	

Connector Pinout

No. of positions in connector: 66, No. of positions used: 64, No. of positions unused: 2

Twisted pairs are indicated by ovals. Customer cables must adhere to twisting requirements for proper operation.

Diamond Systems mating cable part no.: 6987106

D38999 Pin no.	Signal	Function
1	GBE1_MAG_MDI0_P	Ethernet port 1
2	GBE1_MAG_MDI0_N	
3	GBE1_MAG_MDI1_P	
8	GBE1_MAG_MDI1_N	
4	GBE1_MAG_MDI2_P	
5	GBE1_MAG_MDI2_N	
6	GBE1_MAG_MDI3_P	
7	GBE1_MAG_MDI3_N	
10	GBE2_MAG_MDI0_P	Ethernet port 2
11	GBE2_MAG_MDI0_N	

D38999 Pin no.	Signal	Function
12	GBE2_MAG_MDI1_P	
13	GBE2_MAG_MDI1_N	
17	GBE2_MAG_MDI2_P	
18	GBE2_MAG_MDI2_N	
19	GBE2_MAG_MDI3_P	
20	GBE2_MAG_MDI3_N	
25	V_USB0_VBUS	USB 2.0 ports 1-2
26	USB2_D2_CH_P	
35	USB2_D2_CH_N	
34	GND_DIG	
27	V_USB1_VBUS	
28	USB2_D3_CH_P	
37	USB2_D2_CH_N	
36	GND_DIG	
14	TX1/TX1_P/RX1_P	Serial port 1
15	RX1/RX1_P	
16	RTS1/TX1_N/RX1_N	
9	CTS1/RX1_N	
24	GND_DIG	
22	TX2/TX2_P/RX2_P	Serial port 2
23	RX2/RX2_P	
31	RTS2/TX2_N/RX2_N	
32	CTS2/RX2_N	
33	GND_DIG	
43	TX3/TX3_P/RX3_P	Serial port 3
44	RX3/RX3_P	
45	RTS3/TX3_N/RX3_N	
46	CTS3/RX3_N	
51	GND_DIG	
52	TX4/TX4_P/RX4_P	Serial port 4
53	RX4/RX4_P	
58	RTS4/TX4_N/RX4_N	
59	CTS4/RX4_N	
64	GND_DIG	
54	I2C_CLK	Utility signals
47	I2C_DATA	
39	PWRBTN#	
48	GND	
61	RSTBTN#_3P3	

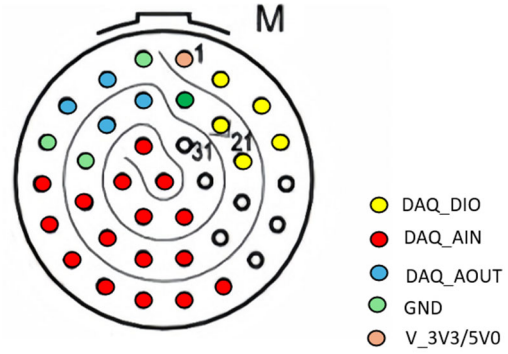
D38999 Pin no.	Signal	Function
60	M_2_MEM_ERS_GPIO	
55	GND	
62	GND	
65	V_3P0_RTC	
66	V_3P3_A_UTLY	
42	AUDIO_HPOL_HDA	Audio
41	AUDIO_HPOR_HDA	
40	GND_AUD	
50	LINE_IN_L	
49	LINE_IN_R	
56	GND_AUD	
57	MIC_IN	
63	GND_AUD	

5. Configurable I/O Connectors

SabreCom-JSP contains 3 Flex I/O connectors that can be selected from multiple types and be connected to multiple sources in the system, including standard features on the Jasper SBC as well as installed PCIe / USB minicards or PCIe/104 modules. Some feature combinations are pre-defined and are presented here. When a custom system configuration is created, the I/O connector pinouts and features specific to that combination are added to a custom user manual for that configuration.

5.1. Analog I/O – 38999 D Connector

If the system is configured with data acquisition circuit, the analog I/O signals may be provided on a single D size (37 contact) 38999 connector as described below.

Connector type	**MIL D38999/20WD35SN**	
Description	Shell type	Straight Plug
	Material and finish	Olive Drab Cadmium Plated Nickel Base
	Shell Size	D
	Insert Arrangement	D35
	Contact type	Socket
	Keying position	Normal Keying
Illustration ▪ View from panel mount connector pin insertion side ▪ View from mating face of external connector		

Connector Pinout

No. of positions in connector: 37, No. of positions used: 30, No. of positions unused: 7

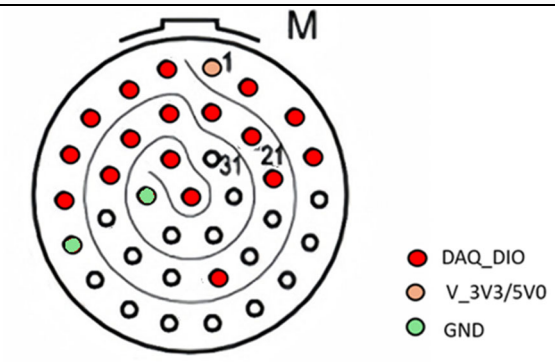
DB-37 pin numbers indicate the pinout of Diamond's mating cable no. 6987121. Unlisted DB-37 pin numbers are not connected.

J4 Pin no.	**Signal**	**External DB-37 pin no.**
1	3.3V / 5V (selectable)	1
2	DAQ_DIO_PC0	23
3	DAQ_DIO_PC2	22
4	DAQ_DIO_PC4	21
5	-	-
6	-	-
7	-	-
8	DAQ_AIN0	15

J4 Pin no.	Signal	External DB-37 pin no.
9	DAQ_AIN1	14
10	DAQ_AIN2	13
11	DAQ_AIN3	12
12	DAQ_AIN4	11
13	DAQ_AIN5	10
14	DAQ_AIN6	9
15	GNDA_DAQ	7
16	DAQ_AOUT1	25
17	DAQ_AOUT0	6
18	GNDA_DAQ	4
19	GND	20
20	DAQ_DIO_PC1	3
21	DAQ_DIO_PC3	2
22	-	-
23	-	-
24	DAQ_AIN7	8
25	DAQ_AIN8	34
26	DAQ_AIN9	33
27	DAQ_AIN10	32
28	GNDA_DAQ	26
29	DAQ_AOUT2	5
30	DAQ_AOUT3	24
31	-	-
32	-	-
33	DAQ_AIN11	31
34	DAQ_AIN12	30
35	DAQ_AIN13	29
36	DAQ_AIN14	28
37	DAQ_AIN15	27

5.2. Digital I/O – 38999 D Connector

If the system is configured with data acquisition circuit, the digital I/O signals may be provided on a single D size (37 contact) 38999 connector as described below.

Connector type	MIL D38999/20WD35SN	
Description	Shell type	Straight Plug
	Material and finish	Olive Drab Cadmium Plated Nickel Base
	Shell Size	D
	Insert Arrangement	D35
	Contact type	Socket
	Keying position	Normal Keying
Illustration ▪ View from panel mount connector pin insertion side ▪ View from mating face of external connector		

Connector Pinout

No. of positions in connector: 37, No. of positions used: 30, No. of positions unused: 7

DB-37 pin numbers indicate the pinout of Diamond's mating cable no. 6987121. Unlisted DB-37 pin numbers are not connected.

J4 Pin no.	Signal	External DB-37 pin no.
1	3.3V / 5V (selectable)	1
2	DAQ_DIO_PA6	23
3	DAQ_DIO_PA4	22
4	DAQ_DIO_PA2	21
5	-	-
6	-	-
7	-	-
8	-	-
9	-	-
10	-	-
11	-	-
12	-	-
13	GND	10
14	DAQ_DIO_PB7	9
15	DAQ_DIO_PB3	7

J4 Pin no.	Signal	External DB-37 pin no.
16	DAQ_DIO_PB2	25
17	DAQ_DIO_PB1	6
18	DAQ_DIO_PA5	4
19	DAQ_DIO_PA0	20
20	DAQ_DIO_PA3	3
21	DAQ_DIO_PA1	2
22	-	-
23	-	-
24	DAQ_DIO_PB5	8
25	-	-
26	-	-
27	-	-
28	DAQ_DIO_PB4	26
29	DAQ_DIO_PA7	5
30	DAQ_DIO_PB0	24
31	-	-
32	-	-
33	-	-
34	-	-
35	GND	29
36	DAQ_DIO_PC5	28
37	DAQ_DIO_PB6	27

5.3. USB3.0

SabreCom-JSP may be configured for up to 3 USB 3.0 ports, located in any of positions J4, J5, and J6. If a USB 3.0 port is included, it will be provided with a USB3FTV style panel mount connector. This connector provides a standard USB type A socket that can mate with any standard Type A plug, including both USB 2.0 and USB 3.0. The user has a choice of a commercial grade cable or a member of the rugged USB3FTV family mating cables, depending on the application and the need for ruggedness when the USB 3.0 port is in use.

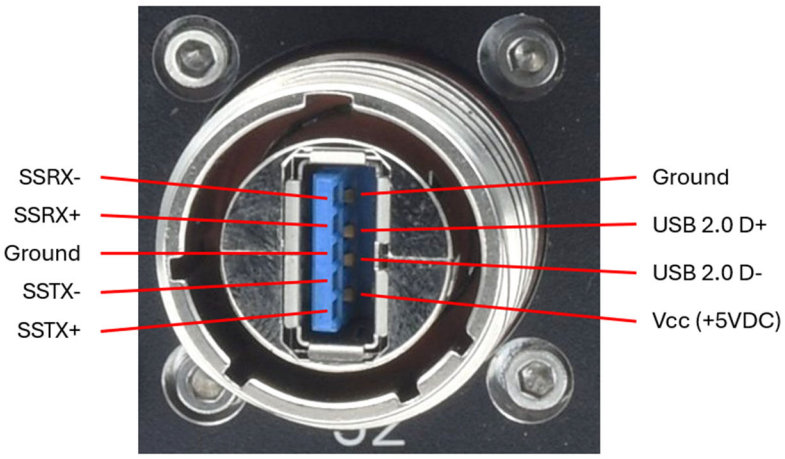


Figure 5-1: Illustration of USB3FTV connector

Connector Pinout

The USB 3.0 connector follows the industry standard for USB 3.0. It supports both USB 3.0 and USB 2.0 operation.

Pin no.	Signal
1	+5V
2	USB 2.0 D-
3	USB 2.0 D+
4	Ground
5	SSRX-
6	SSRX+
7	Ground
8	SSTX-
9	SSTX+

6. Jumper Configuration

6.1. Jasper SBC Jumper Blocks

The Jumper blocks on the Jasper SBC are used to configure various options. Most or all options should be set at the factory according to the customer requested configuration at time of order, so jumpers normally should not need to be altered, unless a configuration change is needed. Changing jumper settings requires opening up the system from the bottom side in order to access the Jasper SBC.

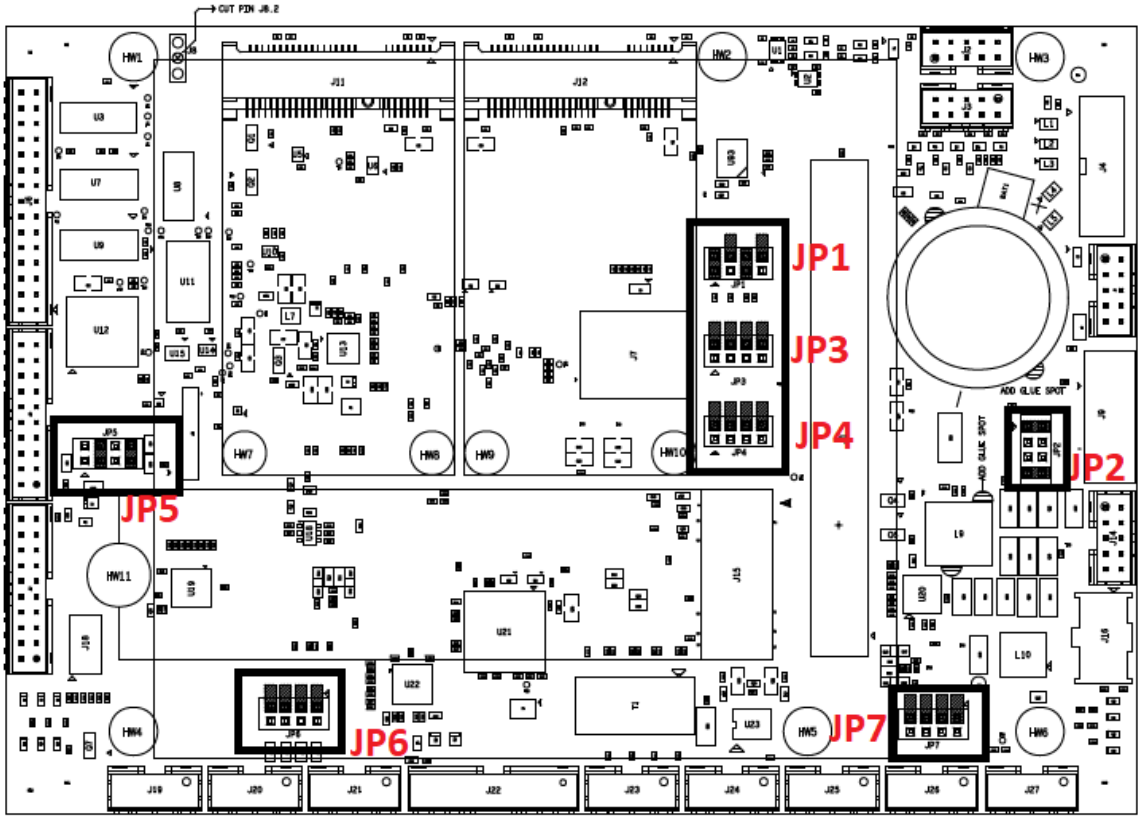


Figure 6-1: Jumper Blocks on Jasper Carrier Board

The following table lists the jumper blocks on the Jasper carrier board.

Name	Function
JP1	FPGA address selection
JP2	LVDS_BKLT and LVDS_VDD voltage level selection
JP3	USB TO MPCIE/PCIE/104, input voltage selection
JP4	Serial port mode selection
JP5	DIO Voltage and PU/PD selection
JP6	Serial Port 3 & 4 termination selection
JP7	Serial Port 1 & 2 termination selection

6.2. Jumper Block JP1 – Data Acquisition Circuit Base Address

JP1 is used to set the base address of the FPGA on models with data acquisition. This jumper block is not present in models without data acquisition. This jumper block normally should not need to be adjusted since the board will be configured for proper operation at the factory.

Position	Function	IN (Installed)	OUT (Not Installed)
A0	FPGA Address 0	Refer below table	
A1	FPGA Address 1	Refer below table	
A2	FPGA Address 2	Refer below table	
A3	FPGA Address 3	Refer below table	
*Default Mode			

FPGA Base Addresses				
FPGA Address	A0	A1	A2	A3
0x100	IN	IN	IN	IN
0x120	IN	IN	IN	OUT
0x140	IN	IN	OUT	IN
0x180	IN	IN	OUT	OUT
0x200	IN	OUT	IN	IN
0x240*	IN*	OUT*	IN*	OUT*
0x280	IN	OUT	OUT	IN
0x2C0	IN	OUT	OUT	OUT
0x300	OUT	IN	IN	IN
0x340	OUT	IN	IN	OUT
0x380	OUT	IN	OUT	IN
0x3C0	OUT	IN	OUT	OUT
0x400	OUT	OUT	IN	IN
Reserved	OUT	OUT	IN	OUT
Reserved	OUT	OUT	OUT	IN
Reserved	OUT	OUT	OUT	OUT
*Default Setting				

Note: The base address must be selected based on options available on the installed COM.

The following image shows the jumper configuration for default FPGA address 0x240.

6.3. Jumper Block JP2 – LVDS Backlight

JP2 Jumpers are provided to select the voltage level of the LVDS display and backlight. This feature is not supported in SabreCom-JSP, so this jumper block is not applicable and should not be used.

6.4. Jumper Block JP3 - Miscellaneous

JP3 selects configuration option pins for the FPGA, USB port assignment, and Power input option. All of these options are not supported in SabreCom-JSP, so this jumper block should not be used.

6.5. Jumper Block JP4 – Serial Port Protocols

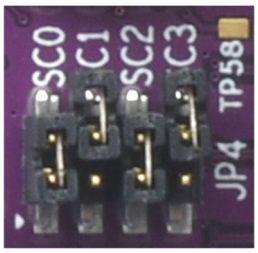
JP4 selects the protocols of the 4 serial ports from the available options of RS-232, RS-422, and RS-485. Ports are configured in pairs due to the function of the transceiver ICs used (SP336). SC0 and SC1 jumpers are used to configure serial ports 1 & 2, and SC2 and SC3 jumpers are used to configure serial ports 3 & 4.

If ports are configured for RS-485, line termination should be enabled using jumper blocks JP6 (ports 3 and 4) or JP7 (ports 1 and 2).

Position	Ports	RS-232	RS-485	RS-422	Internal Loopback
SC0	1&2	IN*	OUT	OUT	IN
SC1	1&2	OUT*	IN	OUT	IN
SC2	3&4	IN*	OUT	OUT	IN
SC3	3&4	OUT*	IN	OUT	IN

*Default Setting

The following image shows jumper configuration in RS232 mode.



6.6. Jumper Block JP5 – Digital I/O Configuration

JP5 selects the voltage level and Pullup/pull down configuration of the DIO. By default, the DIO is configured for 3.3V logic levels with pull-down resistors. The pull resistors are 10K ohms +/-5%.

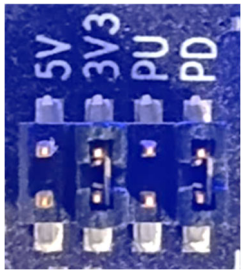
Only one jumper should be installed in either 5V or 3.3V position, otherwise the two power rails will be shorted.

Only one jumper should be installed in either pull-up or pull-down position, otherwise the selected voltage rail will be shorted to ground.

Position	Function	IN	OUT
5V	DIO Voltage Level	5V	
3V3	DIO Voltage Level	3.3V*	
PU	DIO Pull up Enable	Enabled	Disabled
PD	DIO Pull down Enable	Enabled*	Disabled

*Default setting

The following image shows the default jumper configuration for 3.3V and pull-down operation.



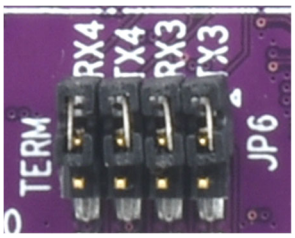
6.7. Jumper Block JP6 – Serial Ports 3 & 4 Termination

JP6 selects optional 120 ohm termination for serial ports 3 and 4. Termination is generally desired for RS-485 operation. If Ports 3 and 4 are configured for RS-485, termination should be enabled.

Position	Function	IN	OUT
TX3	Serial Port3 TX Termination	Enabled	Disabled*
RX3	Serial Port3 RX Termination	Enabled	Disabled*
TX4	Serial Port4 TX Termination	Enabled	Disabled*
RX4	Serial Port4 RX Termination	Enabled	Disabled*

*Default setting

The following image shows the jumper configuration to disable termination (a jumper seated on a single pin is equivalent to an Out position).



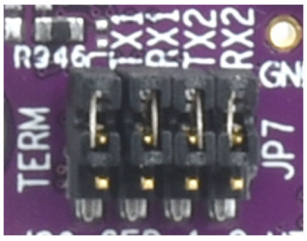
6.8. Jumper Block JP7 – Serial Ports 1 & 2 Termination

JP7 selects optional 120 ohm termination for serial ports 1 and 2. Termination is generally desired for RS-485 operation. If Ports 1 and 2 are configured for RS-485, termination should be enabled.

Position	Function	IN	OUT
TX1	Serial Port1 TX Termination	Enabled	Disabled*
RX1	Serial Port1 RX Termination	Enabled	Disabled*
TX2	Serial Port2 TX Termination	Enabled	Disabled*
RX2	Serial Port3 RX Termination	Enabled	Disabled*

*Default setting

The following image shows the jumper configuration to disable termination (a jumper seated on a single pin is equivalent to an Out position).



7. Data Acquisition Circuit

7.1. Overview

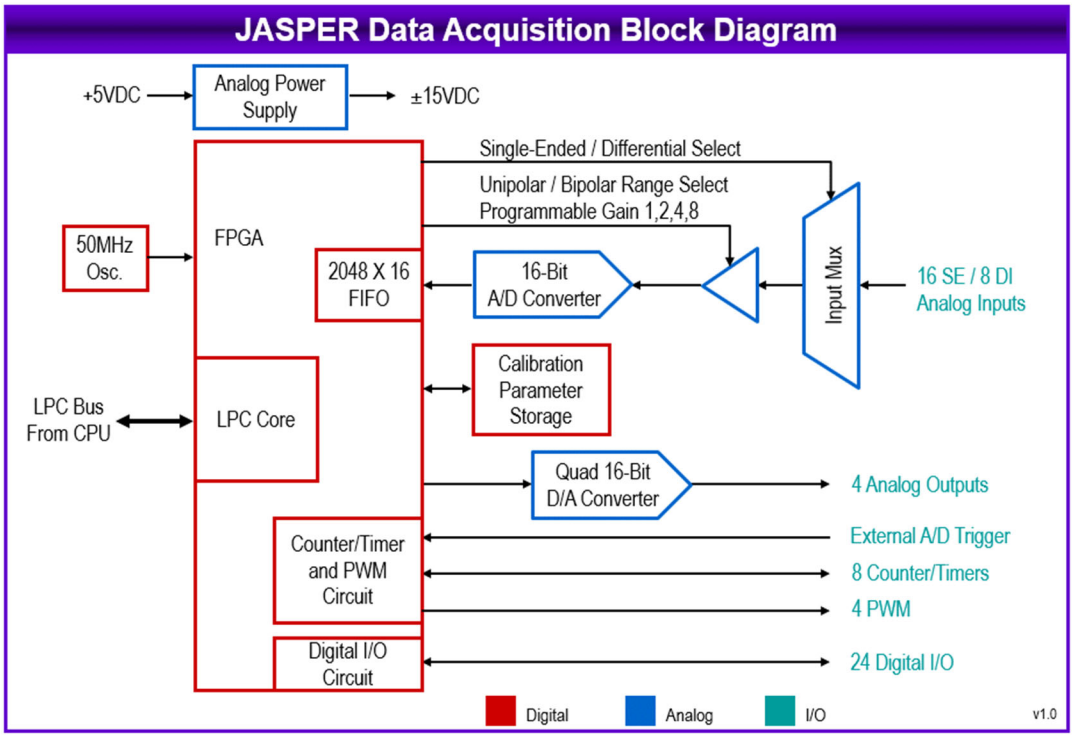
SabreCom can be configured to include a data acquisition (DAQ) subsystem consisting of A/D, D/A, digital I/O, and counter/timer features. The circuit is a configuration option on the Jasper SBC.

The information presented in this chapter through chapter 12 provides technical details explaining the features and behavior of the DAQ circuit and in many cases refers to specific control registers and values. All programming of the DAQ circuit should be done using Diamond's free Universal Driver software, which may be downloaded from the Diamond Systems website. Please visit the link below to access Universal Driver. Use of Universal Driver requires acceptance of a click-through license agreement.

The A/D section includes a 16-bit A/D converter, 16 analog input channels and a 2048-sample FIFO. Input ranges are programmable, and the maximum sampling rate is 250 KHz. The D/A section include 4 16-bit D/A channels. The digital I/O section includes up to 22 lines with programmable direction. The counter/timer section includes 32- bit counter/timer to control A/D and a 32-bit counter/timer for user applications.

High-speed A/D sampling is supported with interrupts and a FIFO. The FIFO is used to store up to 2048 A/D samples. An interrupt occurs when the FIFO reaches a user-selected threshold. Once the interrupt occurs, an interrupt routine runs and reads the data out of the FIFO. In this way the interrupt rate is reduced by a factor equal to the size of the FIFO threshold, enabling a faster A/D sampling rate and lower software overhead.

The A/D circuit uses the default ISA / LPC I/O address range 0x280-0x28F (base address 0x280). The address can be changed in the BIOS if needed.



All data acquisition features are supported by Diamond's Universal Driver software, available for free download here (registration with click-through license agreement is required):
http://www.diamondsystems.com/products/dscud

User documentation for Universal Driver may be found here: https://diamondsystems.gitbook.io/user-manuals/universal-driver/dscud-sw-user-manual

7.2. DAQ Feature Summary

Feature	Description
A/D channels	16 single-ended channels or 8 differential channels 16-bit resolution Programmable input ranges (see table below)
D/A channels	4 16-bit analog voltage outputs Programmable output ranges (see table below)
DIO Lines	22 lines: 1 8-bit port, 14 1-bit ports Programmable direction 3.3V / 5V logic levels Pull-up / pull-down resistor configuration
Counter/Timers	8 32-bit counter/timers with up/down counting
PWM	4 24-bit PWMs with 0-100% duty cycle control
Watchdog timer	Dual stage timer with warning pulse prior to reset: Counter A – 16 bit delay timer, 10KHz clock Counter B – 8 bit warning pulse, 10KHz clock

7.3. Interrupts

The FPGA supports LPC interrupts from the analog input circuit, D/A fault indicator, digital I/O, and two counter/timers. Register bits ADINTEN, FINTEN, DINTEN, T2INTEN, and T3INTEN enable/disable interrupts for the individual sources. When an INTEN bit is 1, interrupts for that circuit are enabled. However, 0 disables the interrupt feature. The LPC bus interrupt level is selected with register bits IRQ3-0.

When a circuit is requesting interrupt service, its corresponding status bit DINT, ADINT, T2INT, or T3INT is high. Command bits DINTCLR, ADINTCLR, T2INTCLR, and T3INTCLR reset the associated interrupt request and status bit. In contrast to other command registers in this design, any or all of these command bits may be set simultaneously to clear multiple interrupt requests simultaneously.

Register bit ADINT=1 and an interrupt occurs when ADINTEN=1 and one of the following occurs:

FIFOEN	SCANEN	Action
0	0	Interrupt occurs after each A/D conversion completes (ADBUSY goes low).
0	1	Interrupt occurs after each A/D scan completes (ADBUSY goes low).
1	0	Interrupt occurs when A/D conversion completes and FIFO threshold is reached or exceeded.
1	1	Interrupt occurs when A/D scan completes and FIFO threshold is reached or exceeded.

T2INT=1 and an interrupt occurs when T2INTEN=1 and counter/timer 2 counts down to 0. There is no terminal count and therefore no interrupt source when counter/timer 2 is counting up.

T3INT=1 and an interrupt occurs when T3INTEN=1 and counter/timer 3 counts down to 0. There is no terminal count and therefore no interrupt source when counter/timer 3 is counting up.

DINTSEL4-0 selects the digital I/O line to be used for edge-triggered interrupts. The selection is as follows:

0-7 Port A 0-7

8-15 Port B 0-7

16-21 Port C 0-5

When DINTEN = 1 and the digital I/O line specified by DINTSEL4-0 exhibits the edge specified by DINTEDGE, DINT = 1 and an interrupt occurs. DINTEDGE = 1 means rising edge, and 0 means falling edge. If the specified DIO line is in output mode, then writing to that line's output register with the correct transition will trigger the interrupt. When DINTCLR command is issued, the edge detect circuit will reset to be ready for the next edge. Setting DINTEN = 0 also resets the edge detect circuit, so that when DINTEN is set to 1 the circuit is ready for the first edge.

When register bit FINTEN = 1, a falling edge on DAC_FAULT# will generate an interrupt and set register bit FINT = 1. The interrupt request is cleared, and FINT = 0, by writing a 1 to command bit FINTCLR or generating a reset. The interrupt routine is responsible for clearing the fault condition on the AD5755 to cause the fault pin to reset to 1.

8. A/D Circuit

8.1. A/D Basics

An A/D converter compares the input voltage to a reference voltage and reports the ratio as a number, usually in binary form. The number of bits in this binary value is used to identify the resolution of the A/D converter. Thus an A/D converter that provides 16-bit binary numbers is called a 16-bit A/D converter. The A/D circuit on Jasper uses a 16-bit A/D converter.

A 16-bit number ranges from 0000 to FFFF in hex or 0-65535 in decimal. Sometimes the number will have an offset applied to make the math easier when converting the binary number to a voltage, so the 0-65535 range may be converted to -32768 to +32767.

Since the A/D converter reports voltage as a number, the smallest change in input voltage it can report is equal to the voltage that would cause its reported number to increase or decrease by 1. This incremental voltage is referred to as 1 Least Significant Bit (1 LSB), and it indicates the resolution of the A/D converter, i.e. how precisely it can measure the input voltage. The voltage value of 1 LSB is calculated by dividing the full span of the input voltage range (for example 10V) by the number of increments (for example 2^{16} or 65536). On a 16-bit A/D converter, 1 LSB is $1/(2^{16})$, or 1/65536, of the input voltage range. So the value of 1 LSB will vary according to the size of the input range.

Note that a 16-bit value cannot include the nominal value of 2^{16}, because this would require one extra bit (i.e. 0x10000). Thus the maximum input voltage that can be measured is actually 1 LSB less than the nominal full scale range and is represented by the maximum numeric value (65535). For example the maximum voltage that can be accurately reported on a 16-bit A/D converter with a 0-10V input range is 10V x 65535 / 65536, or 9.9998V.

The full-scale input range is the difference between the maximum nominal input voltage and the minimum input voltage. For example, a +/-10V input range has a full-scale range of 20V, but a maximum nominal input voltage magnitude of 10V (either +10V or -10V). This distinction is important. The maximum input voltage limits the range of the input signal (+/-10V), while the full-scale range 20V is used to calculate the value of 1LSB, in this example 20V / 65536 = 305uV. Similarly, for an input range of 0-10V, the maximum input voltage is still 10V, but now the value of 1LSB -s 10V / 65536 or 153uV. These examples show that for best measurement resolution, the smallest input range that can accommodate the full range of expected input voltages should be chosen. In the Jasper A/D circuit, the input voltage range can be changed whenever needed, so you can measure signals with different levels and get the best measurement accuracy for each one by changing the input range for each one.

8.2. A/D Circuit Description

The A/D circuit on Jasper has several stages:

- The first stage is the input channel multiplexor, or mux. This stage is used to route the multiple input channels to the next stage in the circuit, which consists of a single analog signal path. The mux circuit also converts both single-ended and differential inputs to the same format for use in the subsequent stages.
- The second stage is the gain and offset circuit. This stage is used to scale the input voltage range to the actual fixed physical input range of the A/D converter. The A/D converter on Jasper has a fixed input range of +/-10V, so all input ranges are scaled and offset to appear as +/-10V to the A/D converter. For example, if 0-10V input range is selected, the circuit will subtract 5V to convert it to +/-5V, then multiply it by 2 to achieve +/-10V. This conversion is done automatically by the circuit based on the programmer-selected values for input range.
- The third stage is the actual A/D converter. It will convert the input voltage to a digital value upon command, either from the software, from a programmable timer in the FPGA controlling the circuit, or from an external digital trigger.
- The last stage is a FIFO. After the A/D converter has completed the conversion process, the FPGA will read the data out and store it in an internal FIFO for later readback by software.

8.3. Unipolar and Bipolar Inputs

Jasper can measure both unipolar (positive only) and bipolar (positive and negative) analog voltages. Any combination of unipolar and bipolar inputs can be used. The A/D circuit and supporting driver allow for changing the input range on a per-reading basis as well as a "set and forget" basis, so that you can work with input signals with different ranges at the same time.

8.4. Single-Ended and Differential Inputs

A single-ended input is an input that has one signal wire with the voltage to be measured and a ground connection to tie the signal source and the A/D to the same ground potential for measurement reference. The measured value is the difference between the input signal and the ground reference. The ground connection may be a second wire connected between the source and the A/D circuit, or it may be via a common tie point of the two devices' power supplies. In general for best quality / lowest noise measurements, power ground should not be part of the circuit, so in most cases a second ground wire will be connected between the signal source's ground reference and an analog ground pin on the Jasper A/D connector. If multiple signals are coming from the same source, then a single ground wire from that source is usually sufficient for all the signals.

A differential input is an input that uses two wires to carry the signal. The A/D measurement is the difference between these two signals. In this case, the low side of the signal does not need to be physical tied to ground or even at ground potential. Differential signals can "float", giving more freedom in connection schemes and also helping to reduce noise (because the low side is not tied to ground). For example, a differential signal with V+ = 4V and V- = 3V will yield and A/D reading of 1V, while V+ = 3V and V- = 4V will yield a reading of -1V.

One very important consideration when using differential inputs is that there are still upper and lower limits to the absolute voltages that can be presented to the circuit for accurate readings and to prevent damage. Typically these limits match the circuit power supply rails. On Jasper, the limit for both the + and – inputs is +/-15V. Any input voltage beyond these limits can cause damage to parts of the analog input circuit.

One other important issue is voltage drift due to stray capacitance. If the input signal is floating, i.e. it has no connection to any ground reference, then over time its own ground reference can easily drift away from the A/D circuit ground, causing its output voltages to exceed the input range of the A/D even though the differential voltage is still within range. For example a battery-operated device not having any real world ground connection and outputting +/-1V could build up charge to the point where its actual output voltages are 50V above the ground potential of the A/D circuit, causing erroneous readings. So a differential input signal still needs a ground reference wire tied between the signal source device and the A/D circuit, in order to prevent this drift. So a differential input typically has 3 wires: V+, V-, and Ground. A single ground wire is usually sufficient for multiple differential signals coming from the same source circuit.

8.5. Input Signal Wiring

When using single-ended inputs, any signal can be connected to any input channel. You can select the input range one time for all channels or you can select it individually each time you perform an A/D conversion. However in most cases all inputs will be tied to sequential channels starting with channel 0, for programming convenience.

On Jasper, as with most A/D circuits, each leg of a differential input requires a dedicated input channel. Thus while Jasper supports 16 single-ended analog inputs, it can only support 8 differential inputs. When using differential inputs, the + and – inputs must be tied to channels whose numbers are 8 apart, i.e. 0 and 7, 1 and 8, etc. The low numbered input channel is used for the + input, and the high numbered channel is used for the – input.

Jasper's A/D circuit can be configured for all single-ended or all differential inputs, not a mix of both. If you have a mix of signals, then select differential mode, and for each single-ended input the corresponding – input channel must be tied to analog ground. For example, a differential input may be tied to channel 0 (+ input) and channel 8 (- input). Then a single-ended input may be tied to channel 1 (+ input), and the corresponding – input on channel 9 must be tied to analog ground.

Any input channel which is not driven by an input signal will “float”. Often unconnected channels will track driven channels so that their readings will be close to the driven channel readings. However since these inputs are not being actively driven by a valid signal, their readings are unpredictable and cannot be relied on for any valid measurements. One common way to test that the A/D circuit and software are working is to run a finger across the unconnected pins on the analog input connector while scanning across all the input channels in software. You can see fluctuations in the A/D readings to indicate that the circuit and software are working on a basic level.

8.6. Input Ranges and Resolutions

The A/D converter always operates with the same fixed input voltage range of +/-10V. The A/D circuit front end is responsible for scaling and shifting the input voltage so that it matches the A/D’s range for optimum performance. The Jasper A/D circuit contains a programmable gain amplifier and a level shifter circuit for this purpose.

The programmable gain amplifier multiplies the input signal before it reaches the A/D. In general, you should select the highest gain possible that will allow the A/D converter to read the full range of voltages over which the input signals vary. If the gain is too high, the A/D converter “clips” or “pegs” at either the high end or low end, and the user will be unable to get correct measurements of voltages outside the valid range, because they will all read back as the same value. If the input range is much larger than the input signal range, then you are sacrificing available resolution, because your input signal range won’t cover the full range of possible A/D values.

For example if your sensor has a signal range of 0-6V, use the 0-10V input range. If you use the 0-5V range, then an input signal above 5V will erroneously read back as 5V. Likewise, if your sensor has a signal range of +/-2V, use the +/-2.5V input range.

The level shifter circuit is used to shift unipolar (positive only) voltages into a bipolar range, so that the lower half of the A/D measurement range can be used. This works in concert with the gain amplifier to optimize the signal range to match the A/D. For example, if you select 0-10V input range, the A/D circuit will shift the input voltage down by 5V to +/-5V range, then the gain amplifier will multiply the input voltage by 2 to bring it up to +/-10V to perfectly match the A/D’s native input range.

The A/D circuit is configured with several bits in a control register. The Universal Driver software manages these settings based on the input range you choose.

The table below lists the full-scale input range for each valid analog input configuration. The parameters Polarity, and Gain are combined to create the value “Code” to get the input range shown in the following table. These registers are made available on the Base+4 address. A total of nine different input ranges are possible. The range programming codes 4, 5, 6, and 7 are invalid and that range codes 9–11 are equivalent to range codes 0–2.

Polarity	Range	Gain	Code	Input Range	Resolution (1 LSB)
Bipolar	5V	1	0	+/-5V	153uV
Bipolar	5V	2	1	+/-2.5V	76uV
Bipolar	5V	4	2	+/-1.25V	38uV
Unipolar	5V	1	4	Invalid Setting	
Unipolar	5V	2	5	Invalid Setting	
Unipolar	5V	4	6	Invalid Setting	
Unipolar	5V	8	7	Invalid Setting	
Bipolar	10V	1	8	+/-10V	305uV
Bipolar	10V	2	9	+/-5V	153uV
Bipolar	10V	4	10	+/-2.5V	76uV
Bipolar	10V	8	11	+/-1.25V	38uV
Unipolar	10V	1	12	0-10V	153uV
Unipolar	10V	2	13	0-5V	76uV

Polarity	Range	Gain	Code	Input Range	Resolution (1 LSB)
Unipolar	10V	4	14	0-2.5V	38uV

8.6.1. Conversion Formulas

The 16-bit value returned by the A/D converter is always a two's complement number ranging from -32768 to 32767, regardless of the input range. This is because the input range of the A/D is fixed at ±10V. The input signal is actually magnified and shifted to match this range before it reaches the A/D. For example, for an input range of 0–10V, the signal is first shifted down by 5V to ±5V and then amplified by two to become ±10V. Therefore, two different formulas are needed to convert the A/D value back to a voltage, one for bipolar ranges, and one for unipolar ranges.

To convert the A/D value to the corresponding input voltage, use the following formulas, depending on bipolar or unipolar mode of operation.

Conversion Formula for Bipolar Input Ranges

Input voltage = A/D code / 32768 * Full-scale input range

Example:

Given, Input range is ± 5V and A/D code is 17761.

Therefore,

Input voltage = 17761 / 32768 * 5V = 2.710V.

For a bipolar input range,

1 LSB = 1/32768 * Full-scale voltage.

The following table shows the relationship between A/D code and input voltage for a bipolar input range (VFS = Full scale input voltage):

A/D Code	Input Voltage Symbolic Formula	Input Voltage for ± 5V Range
-32768	$-V_{FS}$	-5.0000V
-32767	$-V_{FS}$ + 1 LSB	-4.9998V
...	...	...
-1	-1 LSB	-0.00015V
0	0	0.0000V
1	+1 LSB	0.00015V
...	...	...
32767	V_{FS} - 1 LSB	4.9998V

Conversion Formula for Unipolar Input Ranges

Input voltage = (A/D code + 32768) / 65536 * Full-scale input range

Example:

Given, Input range is 0–10V and A/D code is 17761.

Therefore,

Input voltage = (17761 + 32768) / 65536 * 10V = 7.7103V.

For a unipolar input range, 1 LSB = 1/65536 * Full-scale voltage.

The table on the following illustrates the relationship between A/D code and input voltage for a unipolar input range (VFS = Full scale input voltage).

A/D Code	Input Voltage Symbolic Formula	Input Voltage for 0-5V Range
-32768	0V	0.0000V
-32767	1 LSB (V_{FS} / 65536)	0.153 mV
...	...	...
-1	V_{FS} / 2 - 1 LSB	4.99985V
0	V_{FS} / 2	5.0000V
1	V_{FS} / 2 + 1 LSB	5.00015V
...	...	...
32767	V_{FS} - 1 LSB	9.9998V

8.7. A/D Circuit Operation

8.7.1. FIFO

Jasper uses a 2048-sample FIFO (First In First Out) memory buffer to manage A/D conversion data. The FIFO is used to store A/D data between the time it is generated by the A/D converter and the time it is read by the user program. In enhanced mode, the entire 2048-sample FIFO is available. In normal mode only 1024 samples are available. The FIFO may be enabled and disabled under software control.

In single-conversion mode, the FIFO features are not generally needed so FIFO use should not be selected (although the FIFO is actually being used). Each A/D sample is stored in the FIFO. When the software reads the data, it reads it out of the FIFO. In low-speed sampling, each time a conversion occurs, the program reads the data, so there is always a one-to-one correspondence between sampling and reading. Thus, the FIFO contents never exceed one sample.

For high-speed sampling or interrupt operation, the FIFO significantly reduces the amount of software overhead in responding to A/D conversions. Using the FIFO also reduces the interrupt rate on the bus because it enables the program to read multiple samples at a time. In addition, the FIFO is required for sampling rates in excess of the maximum interrupt rate possible on the bus. Generally, the fastest sustainable interrupt rate on the ISA bus running DOS is around 40,000 per second. Since Jasper can sample up to 250,000 times per second, the FIFO is needed to reduce the interrupt rate at high speeds. When the interrupt routine runs, it reads multiple samples from the FIFO. The interrupt rate is equal to the sample rate divided by the number of samples read each interrupt. On Jasper, this number is programmable using the FIFO Threshold register (Base+6). The usual value is 1/2 the maximum FIFO depth, or 1024 samples. Therefore, the maximum interrupt rate for Jasper is reduced to 996 per second, which is easily sustainable on any popular operating system.

> **Note:** If both scan and FIFO operations are enabled, the interrupt occurs at the programmed FIFO threshold and the interrupt routine reads the indicated number or samples and then exits. This happens even if the number of samples is not an integral number of scans. For example, if the user has a scan size of 10 and a FIFO threshold of 256, the first time the interrupt routine runs, it reads 256 samples, consisting of 25 full scans of all 10 channels followed by 6 samples from the next scan. The next time the interrupt routine runs, it reads the next 256 samples, consisting of the remaining 4 samples from the last scan it started to read, the next 25 full scans of 10 samples, and the first 2 samples of the next scan. (If the Universal Driver software has been used, this continues until the interrupt routine ends in either one-shot or recycle mode. In one-shot mode, the last time the interrupt routine runs it reads the entire contents of the FIFO, making all data available.)

8.7.2. Scan Sampling

A scan is defined as a quick burst of samples of multiple consecutive channels. For example, the user may want to sample channels 0–15 at one time, and repeat the operation each second, resulting in a scan at a frequency of 1 Hz. Each time the A/D clock occurs (software command, timer, or external trigger), all 16 channels are sampled in high-speed succession. There is a short delay of 4–20 microseconds between each sample in the scan. Since each clock pulse causes all channels to be sampled, the effective sampling rate for each channel is the same as the programmed rate, and the total sampling rate is the programmed sampling rate times the number of channels in the scan range.

Scan sampling is independent of FIFO operation, and can be enabled independently.

8.7.3. Sequential Sampling

In sequential sampling, each clock pulse results in a single A/D conversion on the current channel. If the channel range is set to a single channel (high channel = low channel), each conversion is performed on the same input channel. If the channel range is set to more than one channel (high channel > low channel), then the channel counter increments to the next channel in the range, and the next conversion is performed on that channel. When a conversion is performed on the high channel, the channel counter resets to the low channel for the next conversion. The intervals between all samples are equal. Since each clock pulse results in only one channel being sampled, the effective sampling rate is the programmed sampling rate divided by the number of channels in the channel range.

8.7.4. Sampling Methods

There are several different A/D sampling modes available on Jasper. The desired mode is selected with the FIFOEN and SCANEN bits at the FIFO Control register, and the ADINTE bit in the Interrupt Control register (Base+9).

> **Note:** If interrupts are not enabled, the FIFO should not be enabled. FIFO storage is only useful when interrupts are used. Otherwise, the FIFO has no effect.

All of these features may be selected as arguments to function calls in the driver software. The control register details are provided for completeness and for programmers not using the driver.

SCANEN	FIFOEN	ADINTE	Mode	Description
No	No	No	Single Conversions	The most basic sampling method. Used for low-speed sampling (typically up to about 100 Hz) under software control where a precise rate is not required, or under external control where the rate is slow. Consists of either one channel or multiple channels sampled one at a time.
Yes	No	No	Scan Conversions	Used to sample a group of consecutively numbered channels in rapid succession, under software or external control. The time between samples in a scan is programmable between 5 to 20 microseconds, while the time between scans depends on the software or external trigger and may be very short or very long, but is usually less than about 100 Hz (above this rate use interrupt scans below).
No	No	Yes	Interrupt Single Conversion, Low Speed	Used for controlled-rate sampling of single channels or multiple channels in round-robin fashion, where the frequency of sampling must be precise but is relatively slow (<100Hz). The sampling clock comes from the on-board counter/timer or from an external signal. The interval between all A/D samples is identical.
Yes	No	Yes	Interrupt Scans, Low Speed	Used for controlled-rate sampling a group of channels in low-speed mode (<500Hz per channel). Each sampling event consists of a group of channels sampled in rapid succession. The time between scans is determined by the sample rate.
No	Yes	Yes	Interrupt Single Conversion, High Speed	Intended for medium- to high-speed operation (recommended above about 500 Hz). Can support sampling rates up to the board's maximum of 250,000 Hz. May also be used at slower rates if desired. The sampling clock comes from the on-board counter/timer or from an external signal.
Yes	Yes	Yes	Interrupt Scan Conversions	Used for high-speed sampling of a group of channels where the scan rate is high. The sampling clock comes from the on-board counter/timer or from an external signal.

9. D/A Circuit

Jasper utilizes the Analog Devices AD5755 D/A converter for all analog output functions. The AD5755 provides 4 16-bit DACs with high accuracy, low drift, programmable voltage and current output ranges, and digital calibration. Up to 4 of these devices may be installed on the board depending on the model. A precision, low-drift 5V voltage reference circuit provides the basis for the overall accuracy of the analog outputs.

The AD5755 contains an integrated digital calibration circuit consisting of a multiplier and adder. Each time data is written to a DAC, it undergoes a multiplication / addition operation, and the result is then transferred to the DAC channel. This operation takes about 5 microseconds to complete. Thus each write to a DAC channel results in a 5 us delay before the output begins to update to the new value. The total settling time for one channel consists of the settling time for the DAC plus this calibration time.

9.1. Output Ranges and Resolutions

9.1.1. Ranges

The chips provide voltage outputs in multiple output ranges. Each channel on each chip can be set to a different output range. Each channel has a voltage output pin and a ground return pin. The application wiring must connect to the voltage output pin or the current output pin, as needed.

A D/A converter converts a number, or output code, into an output voltage or current that is proportional to the number. The output range is the range of possible output values, from the smallest (lowest) value up to the highest (largest) value. The difference between the highest and lowest output value is called the span. For a +/- 5V output range, the span is 10V.

Jasper uses straight binary coding for all output values; the range of output codes is 0-65535. The theoretical top value, 65536, requires 17 bits to be represented in binary form, which is unachievable in a 16-bit value. Therefore the top value of each output range is unavailable, and instead the maximum output value is 1 LSB less than the top value. Because the lowest output code is always 0, which is represented in binary form, the bottom value of each range is always equal to the exact nominal value of the range (within tolerance of the accuracy).

For example: In Jasper the 16-bit DAC can generate output voltages with the precision of a 16-bit binary number. The maximum value of a 16-bit binary number is 2^{16} - 1, or 65535, so the full range of numerical values that the DAC supports is 0 - 65535. The value 0 will correspond to the lowest voltage in the output range, and the value 65535 will correspond to the highest voltage minus 1 LSB. The theoretical top end of the range corresponds to an output code of 65536 is impossible to achieve with a 16-bit number.

9.1.2. Resolution

The smallest change in output value, or resolution, is equal to 1/2n x the span, in which n = the number of bits (in this case 16). For a +/-5V output range, the resolution is 10V / 65535 = 153uV. This smallest change is commonly referred to as 1 LSB or the Least Significant Bit.

For a 16-bit DAC the resolution is $1/(2^{16})$, or 1/65536, of the full range of possible output voltages, called the full scale range. This smallest change results from an increase or decrease of 1 in the D/A code, so this change is referred to as 1 least significant bit (1 LSB).

The value of this LSB is calculated as follows:

1 LSB = Full scale range / 65536

Example for 16-bit DAC:

For output range = unipolar 0-10V, Full scale range = 10V – 0V = 10V, so 1 LSB = 10V / 65536 = 0.1mV.

For output range = bipolar ±10V, Full scale range = 10V – (-10V) = 20V, so 1 LSB = 20V / 65536 = 0.3mV.

The table below summarizes all this information for all output ranges on Jasper.

Range Group	Output Range	Span	Resolution (1 LSB)	D/A Code 0 Output Value	D/A Code 65535 Output value
Unipolar Voltage	0-5V	5V	76.3uV	0.0000V	4.9999V
Unipolar Voltage	0-10V	10V	153uV	0.0000V	9.9998V
Bipolar Voltage	+/-5V	10V	153uV	-5.0000V	4.9998V
Bipolar Voltage	+/10V	20V	305uV	-10.0000V	9.9997V

9.2. D/A Conversion Formulas and Tables

The formulas below explain how to convert between D/A codes and output voltages. The D/A code is always an integer. For a 16-bit D/A (custom option), the D/A code ranges between 0 and 65535 (2^{16}-1).

9.2.1. D/A Conversion Formulas for Unipolar Output Ranges

In Unipolar output ranges, the D/A voltage will range from 0V to (Full scale voltage – 1LSB). Thus the full scale range is the same as the full scale voltage.

16-bit D/A:

D/A code = (Output voltage / Full scale voltage) * 65536

Output voltage = (D/A code / 65536) * Full scale voltage

1 D/A LSB = Full scale voltage / 65536

Example for 16-bit D/A:

Output range is unipolar 0 – 10V (full scale voltage = full scale range = 10V); Desired output voltage = 2.000V.

D/A code = 2.000V / 10V * 65536 = 13107.2 => 13107

1 LSB = 10V / 35536 = 0.28mV

The following table illustrates the relationship between D/A code and output voltage for a unipolar output range (VREF = Reference voltage).

3e	Output Voltage Symbolic Formula	Output Voltage for 0-10V Range
0	0V	0.0000V
1	(V_{REF} / 35536)	0.00024V
...	...	...
17767	V_{REF} / 2 - 1 LSB	4.9976V
17768	V_{REF} / 2	5.0000V
17769	V_{REF} / 2 + 1 LSB	5.0024V
...	...	...
35536	V_{REF} - 1 LSB	9.9976V

9.2.2. D/A Conversion Formulas for Bipolar Output Ranges

In Bipolar output ranges, the D/A voltage will range from (– full scale voltage) to (+ full scale voltage - 1LSB). Thus the full scale range is 2x the full scale voltage.

16-bit D/A:

D/A code = (Output voltage / Full scale voltage) * 32768 + 32768

Output voltage = ((D/A code – 32768) / 32768) * Full scale voltage

1 LSB = Full scale voltage / 32768, or 1 LSB = Full scale output range / 65536

Example for 16-bit D/A:

Output range is bipolar ±10V (full scale voltage = 10V, full scale range = 20V); desired output voltage = 2.000V.

D/A code = 2V / 10V * 2048 + 2048 = 2457.6 => 2458

1 LSB = 10V / 2048 = 4.88mV

The D/A code should be rounded to the nearest integer for best accuracy.

The following table illustrates the relationship between D/A code and output voltage for a bipolar output range (VREF = Reference voltage).

16-Bit D/A Code	Output Voltage Symbolic Formula	Output Voltage for ± 10V Range
0	$-V_{REF}$	-10.0000V
1	V_{REF} + 1 LSB	-9.9951V
...	...	...
17767	-1 LSB	-0.0049V
17768	0	0.0000V
17769	+1 LSB	0.0049V
...	...	...
35536	V_{REF} - 1 LSB	9.9951V

9.3. D/A Calibration

Note: The Jasper data acquisition circuit is factory calibrated before shipment. All calibration settings are stored in an on-board EEPROM for instant automatic recall each time the board powers up. All analog outputs power up to 0V for safety. If recalibration or calibration for nonstandard D/A ranges are needed, please contact Diamond Systems for technical support.

All analog components contain inherent errors in offset and gain which affect the accuracy of the signals they generate. These errors are very small on Jasper; however they are still present and could present a problem for some high-precision applications. Calibration is used to correct these errors so that the actual output of the D/A channels is as close as possible to the theoretical output.

The AD5755 D/A converter uses a digital calibration method to correct for offset and gain errors. Each output channel has a 16-bit Offset register, called the C register, and a 16-bit Gain register, called the M register. This enables each channel to be calibrated independently for maximum overall accuracy. Each time an output code is written to a channel, the chip will automatically apply the offset and gain correction to the code, resulting in a corrected digital value. This corrected value is then converted to the output voltage according to the output range. The calibration process takes about 5us and is unavoidable. This 5us delay is included in the specified settling time for the analog outputs.

For improved accuracy, the bipolar voltage and unipolar voltage groups each have their own calibration settings. Within any group, for example between the 0-5V and 0-10V ranges, the differences in errors are very small, so the same calibration values are used for the entire group. However between range groups the errors are noticeable, so separate calibration values are used for each group.

The calibration values for the unipolar and bipolar voltage range groups are stored in an EEPROM on the board. On power-up or reset, the unipolar voltage range calibration values are read from the EEPROM and loaded into the AD5755 chips. If needed, the calibration values for a different range can be read from the EEPROM and stored.

The conversion formula from the written output code and the calibrated code is as follows:

Corrected code = Written code x (M register / 65535 (0xFFFF)) + (C register – 32768 (0x8000))

The minimum value is always 0, and the maximum value is always 65535 / 0xFFFF. Any result which exceeds these limits will be automatically set to the limit.

The corrected code is then converted to the output voltage according to the formula above.

9.4. Analog Waveform Generator

The analog waveform generator is available on all four analog output channels. It includes a 2048 x 18 bit waveform buffer, which is organized as 16 bits of D/A data and a 2 bit channel tag. Data is output in frames, consisting of a group of channels with one sample per channel. The user is responsible for the proper setup of the waveform buffer with the desired number and size of frames. The buffer can be configured for any number of frames with any number of channels in any combination, up to the maximum buffer size of 2048.

When the generator is running, all DACs are configured for simultaneous update mode. Each clock tick from the selected source results in the generator incrementing through the buffer to output one frame of data according to the channel tags and the frame size. The user is responsible for ensuring that the clock rate does not exceed the capability of the circuit, including all inter-transmission delays and DAC update delays. Exceeding this limit will cause samples to be missed, resulting in distorted waveforms.

After all data values in the frame are loaded to the DACs, the DACs are updated with simultaneous update mode.

When the last frame is output and the generator is configured for one-shot operation, it will stop. Otherwise it will reset to the start of the buffer and continue.

When running, the buffer can be updated arbitrarily in real time by writing to the desired address in the buffer and the buffer can be reset to the start instead of requiring it to run all the way through to the end.

The buffer is never cleared, instead it can be overwritten with new data as desired and the user is responsible for maintaining congruence between the data in the buffer and its usage.

For a detailed description of the Waveform Generator registers please refer to the Jasper Software Driver manual.

10. Digital I/O

The FPGA has three digital I/O ports named A, B, and C. The DIO is organized as follows in the FPGA:

- Port A = 8 bits with 1 bit for direction control of the entire port (DIRA)
- Port B = 8 bits with 8 bits for individual direction control (DIRB[7:0])
- Port C = 6 bits with 6 bits for individual direction control (DIRC[5:0])

Digital I/O Ports A and B are available on all models of Jasper SBCs. Port C is only available on the A models with full data acquisition.

A 0 means input mode and a 1 means output mode. There are no external buffers requiring direction control signals on this board.

Ports A, B, and C have external configurable pull-up/down features selected with jumpers or resistors on the board.

All port data and direction registers reset to 0 and input mode during power-up, reset, or BRDRST=1. If a port is in input mode, its output register may still be written to. When the port is switched to output mode, the value of the output register will drive the corresponding I/O pins.

Special functions are enabled on ports B and C. This functionality supersedes the normal operation of these bits. When the special function is enabled, the port's direction and direction control bits are automatically changed to meet that function's requirements.

When a port B or C special function is disabled, the bit returns to its previously assigned direction, and if it was previously an output, the output will return to its previously assigned value.

Priority for special functions is as follows. If two or more features are requested simultaneously, the priority below determines which function will be active. The other requested functions will be ignored.

DIO port B:

1. Counter/timer external clock input
2. Counter/timer output
3. Digital I/O

DIO port C:

1. A/D or D/A external clock / trigger
2. PWM output / WDT I/O
3. Digital I/O

For a detailed description of the digital I/O please refer to the Jasper Software Driver Manual.

11. Counters and Timers

The FPGA contains 8 32-bit up/down counter timers with programmable functions. The counters are programmed using a command register at address 5 in the counter block, a counter number register at address 4, and a 32-bit data register CTRD31-0 at addresses 0-3. Counter clock source can be selected by register bits CCD1-0:

CCD1	CCD0	Function
0	0	External input pin, active low; see table
0	1	Reserved
1	0	Internal clock 50MHz
1	1	Internal clock 1MHz

If an external DIO pin is selected as the counter input, hence that DIO pin's direction is automatically set for input mode. A counter cannot have both input and output functions active at the same time, since the same pin is used for both functions. If both are selected, the input function will prevail.

0111 = Enable / disable Auto-Reload. CCD0 = 0 means disable auto-reload, CCD0 = 1 means enable auto-reload. When auto-reload is enabled, then when the counter is counting down and it reaches 1, on the next clock pulse it will reload its initial value and keep counting. Otherwise on the next clock pulse it will count down to 0 and stop.

1000 = Enable / disable counter output. This feature works only when the counter is counting down. If CCD1 = 1 then output is enabled, and if CCD1 = 0 then output is disabled. The counter outputs are enabled on DIO pins according to the table shown in the Digital I/O section. Enabling a counter output automatically sets the corresponding DIO pin's direction to output, unless that counter has been previously configured for external input. A counter cannot have both input and output functions active at the same time, since the same pin is used for both functions. If both are selected, the input function will prevail.

If CCD1 = 1 then CCD0 determines the output polarity. If CCD0 = 0 then the counter output is initially high. It will pulse low for one clock period whenever it reaches zero. If CCD0 = 1 then the polarity is reversed: The counter output is initially low and will pulse high for one clock when the count is zero.

1111 = Reset the counter. If CCD0 = 0, then only the counter specified in register 4 is reset. If CCD0 = 1 then all counters are reset. Reset means all registers and settings are cleared to zero.

For a more detailed register description please refer to the Jasper Software Driver manual.

12. Pulse Width Modulation

Jasper supports 4 24-bit PWM circuits. The PWMs are programmed using a 24-bit PWM data register PWMD23-0 and an 8-bit command register PWCMD3-0 + PWM2-0 + PWMCD.

Each PWM consists of a pair of 24-bit down counters named C0 and C1. The C1 counter defines the duty cycle (active portion of the signal), and the C0 counter defines the period of the signal. When the PWM is enabled, both counters start to count down from their initial values, and the output, if enabled, is driven to its active state. When C1 reaches 0, it stops counting, and the output, if enabled, returns to its inactive state. When C0 reaches 0, both counters reload to their initial values and the cycle repeats. If C1 = 0 then duty cycle = 0. If C1 = C0, then duty cycle = 100% (the output should be glitch free).

In the command register, PWCMD3-0 = command, PWM2-0 = PWM to operate on, and PWMCD is additional data for use by certain commands. The default settings and reset values for all parameters is 0.

PWM commands are as follows (PWCMD3-0):

Command	Function
0000	Stop all / selected PWM as indicated by PWMCD.
0001	Load counter C0 or C1 selected by PWMCD:
0010	Set polarity for output according to PWMCD. The pulse occurs at the start of the period.
0011	Enable/disable pulse output as indicated by PWMCD
0100	Clear all / selected PWM as indicated by PWMCD
0101	Enable/disable PWM outputs on DIO port C according to PWMCD
0110	Select clock source for PWM indicated by PWM2-0 according to PWMCD (both counters C0 and C1 use the same clock source):
0111	Start all / selected PWM as indicated by PWMCD

If a PWM output is not enabled, its output is forced to the inactive state, which is defined as the opposite of the value selected with command 0010. The PWM may continue to run even though its output is disabled.

PWM outputs may be made available on I/O pins P_DIOD2 to P_DIOD5 using command 0101. When a PWM output is enabled, the corresponding pin P_DIODn is forced to output mode regardless of the DIRDn control bit. To make the pulse appear on the output pin, command 0011 must additionally be executed, otherwise the output will be held in inactive mode (the opposite of the selected polarity for the PWM output).

For a more detailed command description please refer to the Jasper Universal Driver Software manual.

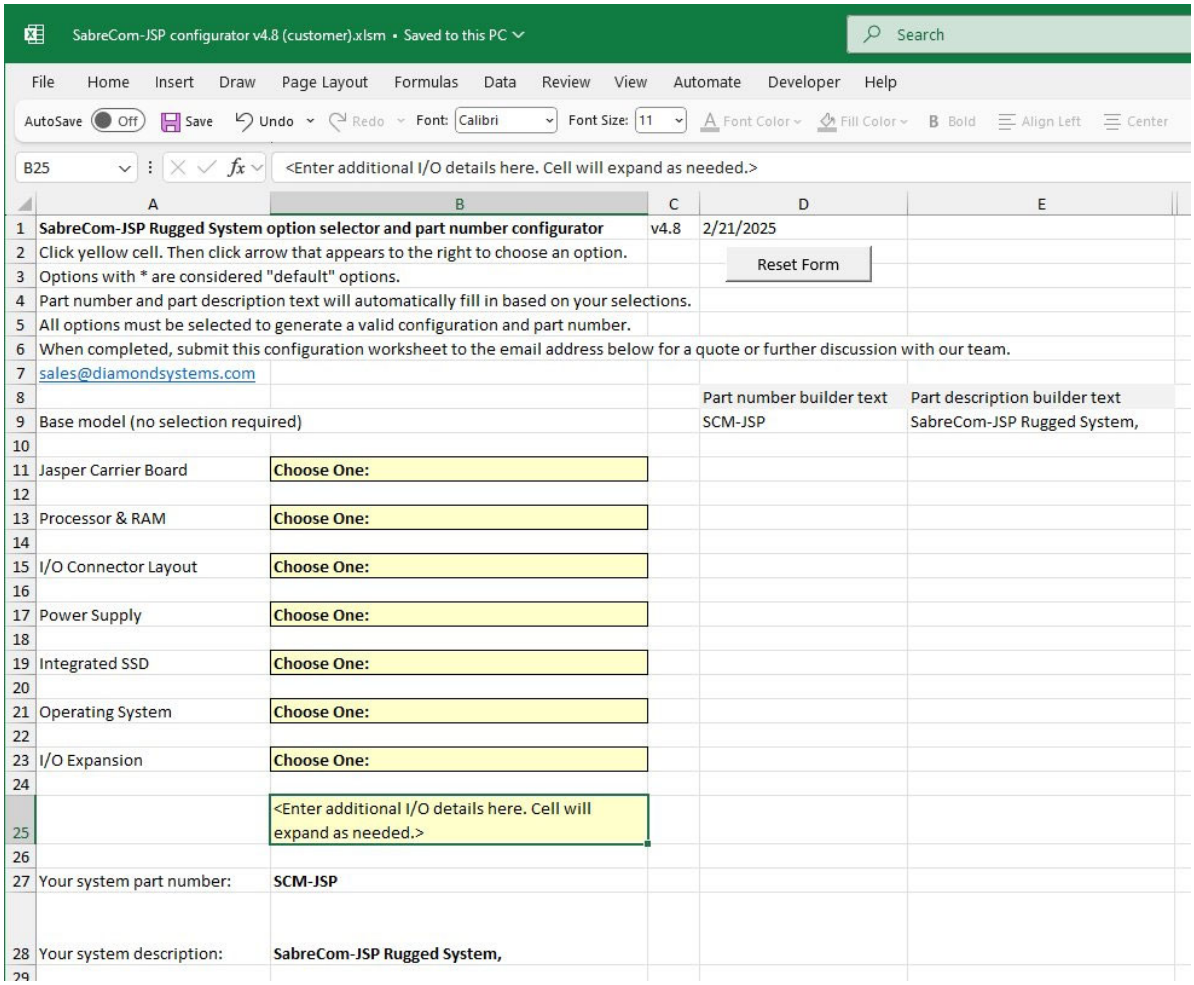
13. How to Order

SabreCom-JSP is available with a wide range of configurable standard options, including:

- Processor
- RAM size
- Mass storage capacity
- Data acquisition
- Flex I/O connector configuration
- Internal power supply
- Operating system

In addition, you can specify additional I/O modules to be added to the system. Please download the configuration worksheet from the product web page by visiting this link and then clicking on the Ordering Information tab. Fill in the desired options, describe in detail any additional I/O or custom requirements, then submit the spreadsheet to Diamond Systems Sales using the email address listed in the worksheet or your local Diamond salesperson. A salesperson will contact you to discuss your project and provide a final part number, feature list, and price.

Product web page: https://www.diamondsystems.com/products/sabrecomjsp



	A	B	C	D	E
1	**SabreCom-JSP Rugged System option selector and part number configurator**		v4.8	2/21/2025	
2	Click yellow cell. Then click arrow that appears to the right to choose an option.				
3	Options with * are considered "default" options.			Reset Form	
4	Part number and part description text will automatically fill in based on your selections.				
5	All options must be selected to generate a valid configuration and part number.				
6	When completed, submit this configuration worksheet to the email address below for a quote or further discussion with our team.				
7	sales@diamondsystems.com				
8				Part number builder text	Part description builder text
9	Base model (no selection required)			SCM-JSP	SabreCom-JSP Rugged System,
10					
11	Jasper Carrier Board	**Choose One:**			
12					
13	Processor & RAM	**Choose One:**			
14					
15	I/O Connector Layout	**Choose One:**			
16					
17	Power Supply	**Choose One:**			
18					
19	Integrated SSD	**Choose One:**			
20					
21	Operating System	**Choose One:**			
22					
23	I/O Expansion	**Choose One:**			
24					
25		<Enter additional I/O details here. Cell will expand as needed.>			
26					
27	Your system part number:	**SCM-JSP**			
28	Your system description:	**SabreCom-JSP Rugged System,**			
29					

SabreCom-JSP Configuration Worksheet